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( ) continuation-in-part application

**INVENTOR(S): Karen Lo, Robert D. Snyder**

**TITLE: HALTING DATA STROBES ON A SOURCE SYNCHRONOUS LINK AND UTILIZATION OF SAME TO DEBUG DATA CAPTURE PROBLEMS**

Enclosed are:

- ☒ The Declaration and Power of Attorney.    ( ) signed    ☒ unsigned or partially signed  
☒ 15 sheets of drawings (one set)    ( ) Associate Power of Attorney  
( ) Form PTO-1449    ( ) Information Disclosure Statement and Form PTO-1449  
( ) Priority document(s) ( ) XOther (fee \$ )

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By

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**HALTING DATA STROBES ON A SOURCE SYNCHRONOUS LINK  
AND UTILIZATION OF SAME TO DEBUG DATA CAPTURE PROBLEMS**

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**RELATED APPLICATIONS**

This application shared a common disclosure with a commonly-owned U.S. Utility Patent Application entitled "A SOURCE SYNCHRONOUS LINK WITH DATA AND CLOCK SIGNALS HAVING THE SAME ELECTRICAL CHARACTERISTICS"

10 naming as inventors Karen Lo, Jeffery A. Benis and Allan R. Desroches, filed concurrently herewith under Attorney Docket No. 10002534-1, the specification of which is herein incorporated by reference.

15

**BACKGROUND OF THE INVENTION**

***Field of The Invention***

The present invention relates generally to source synchronous communication links and, more particularly, to debugging data capture problems on source synchronous communication links.

20 ***Related Art***

Chipsets and other devices communicate over a trace, bus, wire or other communication link or channel. External clocks are often used to synchronize the timing between such communicating components. Typically, with regard to chipsets, an external clock chip generates a system clock that is routed throughout the circuit board to different components for translation into an internal clock. The internal clock is then used by the individual components to generate internal and external signals. The extended routing of the system clock combined with the translation of the system clock to an internal clock by individual components results in timing variations at the interface of the different components. For systems operating at a low frequency most such timing variations can be absorbed by a longer system clock cycle while more extreme timing variations can be bypassed through the addition of wait states to the valid time of a signal.

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Recent advances in microprocessor technology have provided processors with substantially greater operating frequencies. To fully utilize the benefits provided by such microprocessors, system clock speeds must be increased. As the system clock speeds have increased, common-clocked, data transfer systems developed problems such as

5 flight time delays, clock skews, etc.

To overcome these communication problems source synchronous communication techniques have been developed. In a source synchronous environment, clock or strobe signals are sent between components along with the data signals to communicate timing information. Instead of having one or more components operate on a common clock

10 signal, data is communicated at a speed that is not set by a common clock signal. The strobe signal sent with the data may be used, for example, to start an internal clock, for latching of the data, or for other timing purposes. In this way, source synchronous communication eliminates many of the noted problems of traditional, common-clocked, data transfers, thereby providing increased data transfer rates over traditional data

15 transfer schemes.

The term 'data eye' is commonly used to describe the shape of the data waveform as it has a shape resembling a partially closed eye. Typically, the data strobe, which may be a single or two differential signals, is skewed so that it is phase shifted by 90 degrees (centered) with respect to the data signal with which it is sent. That is, a rising or falling

20 edge of the data strobe falls close to the center of the data eye. This guarantees that each data bit is stable at the source synchronous receiver at the time of receipt of the corresponding clock signal, increasing the likelihood that the data will be properly latched into the source synchronous receiver.

Unfortunately, however, a high-speed source synchronous communication link is

25 susceptible to electrical data capture errors. Electrical characteristics of the link such as connector quality, length of trace lines, capacitive and inductive coupling, cross-talk and the like degrade the integrity of the data signal; that is, diminish the size of the data eye. The timing and noise margins of the data signals, which are determined by the width and height, respectively, of the data eye, are likewise decreased. For high-speed

communication links, these reductions, particularly in the timing margin, prevent the communication link from operating at the targeted frequencies.

5 A number of traditional approaches have been suggested to determine whether data capture errors have occurred. One conventional approach has been to use scan-on-the-fly (SOTF) techniques. Such techniques, which are commonly used to capture data located in internal registers in the core of a chip, require the addition of a debug flip-flop coupled to the output of each of the data capture flip-flops. Such shadow flip-flops receive the captured data as it is output from the data capture flip-flop. The captured data can then be made available for subsequent analysis. One drawback to this approach is that since a  
10 debug flip-flop must be coupled to each data capture flip-flop, twice as many flip-flops must be implemented, drastically increasing the requisite area consumed by the receiving device. More importantly, perhaps, is the increased capacitive loading that is placed on the data capture flip-flops, which may be significant depending on the distance between the shadow flip-flop and its corresponding data capture flip-flop. This increased  
15 capacitive loading on the data capture flip-flops increases the latency of the data path, further reducing the timing margins.

Another approach has been to scan the captured data directly from the data capture flip-flops. However, to scan the data from the flip-flops, additional devices such as a multiplexer must be implemented in the functional data path to control the clock  
20 provided to the data capture flip-flops. Such additional components in the functional data path increase the latency of the data path, further reducing the timing margins.

What is needed, therefore, is an apparatus and methodology for optimizing the timing margins of a source synchronous communication link and for determining the data capture capability of a source synchronous link without introducing additional logic, area  
25 or latency in the functional data path.

## SUMMARY OF THE INVENTION

The present invention is directed to methods and apparatus for halting the data strobes transmitted over a source synchronous link to enable the data stored in the data capture flip-flops in a source synchronous receiver to be scanned out for subsequent analysis. Advantageously, this allows for the evaluation of the captured data without placing additional components in the functional data path and, therefore, without increasing the latency of the transmission.

The present invention is also directed to providing optimal timing margins by logically and electrically matching the data and data strobe paths. This includes routing the data and data strobe signals in close proximity from the transmitter to the receiver, and through the same logical and physical elements in the transmitter and receiver. This insures that any injected link noise is experienced common-mode. In addition, the data strobe signal is preferably driven at one-half of the period of the data signal so that the data strobe and data signals experience logical state transitions at the same time and at the same frequency. This insures maximally similar electrical modes on the communication link, further maximizing link margin.

A number of aspects of the invention are summarized below, along with different embodiments that may be implemented for each of the summarized aspects. It should be understood that the embodiments are not necessarily inclusive or exclusive of each other and may be combined in any manner that is non-conflicting and otherwise possible. It should also be understood that these summarized aspects of the invention are exemplary only and are considered to be non-limiting.

In one aspect of the invention a source synchronous link is disclosed. The source synchronous link includes a communication link, a source synchronous receiver; and a source synchronous transmitter. The source synchronous transmitter includes data transmit logic configured to manage the transmission of data signals over a data line of the communication channel. The transmitter also includes data strobe transmit logic configured to generate one or more data strobe signals over a clock line of the communications link. The data strobe transmit logic halts each data strobe signal in a logical state in response to an external condition.

In another aspect of the invention, a source synchronous transmitter is disclosed. The transmitter is constructed and arranged to transmit a differential data strobe over a source synchronous link at a first frequency. The differential data strobe signals are toggling between one of two logical states at a first frequency when operating in a normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in a data capture debug mode of operation.

In a still further aspect of the invention a debug system for determining whether source synchronous receiver has properly captured data transmitted from a transmitter is disclosed. The debug system includes a source synchronous transmitter, a source synchronous receiver; and a debug system. The debug system is configured to control said transmitter to transmit data and a data strobe at a first frequency and to transmit a debug bit pattern while holding said differential data strobe at a predetermined logic level. In addition, the debug system includes a data capture storage and analysis device configured to scan said receiver to retrieve and store captured data for comparison with said debug bit pattern.

In another aspect of the invention, a method for determining whether a source synchronous link receiver properly captured data transmitted by a source synchronous transmitter is disclosed. The method includes the steps of: a) transmitting by the transmitter a data signal at a first clock frequency; b) transmitting by the transmitter concurrently with said step a), at least one data strobe signal at a second clock frequency, wherein said data strobe signal alternates between a high logical state and a low logical state during each data strobe cycle; c) receiving, by the transmitter, a command to halt the data strobe signal; and d) maintaining, by the transmitter in response to said command, said one or more data strobe signals transmitted by said transmitter at one logical state.

In a still further aspect, a method for determining whether a source synchronous receiver has properly captured data transmitted from a source synchronous transmitter is disclosed. The method includes the steps of: selecting a bit pattern to transmit over communication link coupling said transmitter and said receiver; causing the transmitter to halt differential data strobe and to transmit concurrently said predetermined bit pattern to the receiver; scanning data capture flip-flops in the source synchronous receiver to

retrieve captured bit pattern; storing said captured data; and comparing said captured data with said transmitted bit pattern.

In yet another aspect of the invention, a differential data strobe transmitter for generating a differential data strobe comprising a data strobe signal and an inverse data strobe signal over a communication link with a data signal is disclosed. The transmitter includes a differential data strobe signal generator that determines a shape of said data strobe signal and said inverse data strobe signal waveforms; and strobe stopping logic configured to control signal level states used by said signal generator logic to cause said data strobe signal and said inverse data strobe signal to remain halted in a desired logical state.

Various embodiment of the present invention provide certain advantages and overcome certain drawbacks of the above and other conventional techniques. Not all embodiments of the present invention share the same advantages and those that do may not share them under the same or similar circumstances. Further features and advantages of the present invention as well as the structure and operation of various embodiments of the present invention are described in detail below with reference to the accompanying drawings. In the drawings, like reference numerals indicate like or functionally similar elements. Additionally, the left-most one or two digits of a reference numeral identifies the drawing in which the reference numeral first appears.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is pointed out with particularity in the appended claims. The above and further features and advantages of this invention may be better understood by referring to the following description when taken in conjunction with the accompanying drawings, in which:

Figure 1A is a block diagram of two processing cores communicating over a source synchronous link in accordance with aspects of the present invention.

Figure 1B is a block diagram of an exemplary debug system in which aspects of the

present invention may be implemented.

Figure 2A is functional block diagram of one embodiment of differential data strobe transmits logic illustrated in Figure 1A.

Figure 2B is a timing diagram illustrating the relationship between the signals  
5 depicted in Figure 2A.

Figure 3 is a timing diagram illustrating the relationship between processing core control signals and the differential data strobe signals in accordance with one aspect of the present invention.

Figure 4 is a schematic diagram of one embodiment of the pulse stretch logic  
10 illustrated Figure 2A.

Figure 5 is a timing diagram illustrating the operation of the pulse stretch circuit when the strobe stopping logic receives instructions to enter the strobe halting mode of operation.

Figure 6 is a schematic diagram of one embodiment of the differential data strobe  
15 control logic illustrated Figure 2A.

Figure 7 is a timing diagram illustrating the relationship between the signals related to differential data strobe control logic.

Figure 8 is an architectural block diagram of one embodiment of differential data strobe signal generator illustrated in Figure 2A.

Figure 9 is a diagram illustrating the timing relationships between the signals that  
20 appear in Figure 8.

Figure 10 is a schematic block diagram of one embodiment of the source synchronous receiver illustrated in Figure 1.

Figure 11 is an architectural circuit diagram of one embodiment of the data transmit  
25 logic illustrated in Figure 1.



Figure 12 is a timing diagram illustrating the relationship between the signals illustrated in Figure 11.

Figure 13 is a flow chart of one embodiment of the processes performed to halt a differential data strobe in a source synchronous link.

## DETAILED DESCRIPTION

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#### E. Source Synchronous Link Receiver

#### A. Introduction

The present invention is directed to methods and apparatus for halting the data strobes transmitted over a source synchronous link to enable the data stored in the data capture flip-flops in a source synchronous receiver to be scanned out for subsequent analysis. Advantageously, this allows for the evaluation of the captured data without placing additional components in the functional data path and, therefore, without increasing the latency of the transmission.

The present invention is also directed to providing optimal timing margins by logically and electrically matching the data and data strobe paths. This includes routing the data and data strobe signals in close proximity from the transmitter to the receiver, and through the same logical and physical elements in the transmitter and receiver. This insures that any injected link noise is experienced common-mode. In addition, the data strobe signal is preferably driven at one-half of the period of the data signal so that the

data strobe and data signals experience logical state transitions at the same time and at the same frequency. This insures the data and data strobe signals have substantially the same electrical characteristics on the communication link, further maximizing link margins.

- 5           At least one preferred aspect and embodiment of the present invention is described in detail below. While specific configurations are provided, it should be understood that such configurations are illustrative only and that other components, configurations and operations may be implemented without departing from the scope of the present invention.

10       **B. Exemplary Source Synchronous Link Environment**

- Figure 1A is a block diagram of two processing cores communicating over a source synchronous link 100 in accordance with aspects of the present invention. A first processing node or core 102 includes a source synchronous transmitter 108 and a second processing node or core 104 includes a source synchronous receiver 110. Source  
15       synchronous transmitter 108 and source synchronous receiver 110 are connected via a communication channel or link 106. Data is transferred across link 106 along with an accompanying clock. This is referred to generally as a source synchronous link 106.

- Source synchronous transmitter 108 and receiver 110 include input and output (I/O) cells and driver and receiver logic connected to a system level interconnect such a printed  
20       circuit board trace. The input and output cells act as an interface between the driver and receiver and the printed circuit board interconnect. Such devices are considered to be well-known in the art and are not described further herein.

- Source synchronous transmitter 108 generally includes data transmit logic 112 and differential data strobe transmit logic 114. Data transmit logic 112 manages the  
25       transmission of data signals 120 over a data line of source synchronous link 106. Differential data strobe transmit logic 114 generates a differential clock or data strobe signal over two clock lines of source synchronous link 106. Source synchronous transmitter 108 receives a local or core clock 116 and, in certain aspects of the invention, a second local or core clock 118. As will be described in detail below, the second clock

may be generated internally by transmitter 108 and need not be implemented in all aspects of the present invention.

In one embodiment each processing core 102, 104 has both a transmitter 108 and receiver 110. Accordingly, each processing core can be both driving data to, and receiving data from, another processing core concurrently; that is, the communication link 106 is full duplex. In the disclosed embodiment, the clock signal that is transmitted with the data signals is referred to as a data strobe and is sent differentially. That is, there are two clock lines for the data strobe between transmitter 108 and receiver 110, each line having an inverse clock or strobe signal of the other. As such, the exemplary embodiments of the invention presented herein include what is referred to as a differential data strobe. As will be described in detail below, the two data strobe signals are used to latch data into receiver 110 on both edges of the clock cycle. However, it should be understood that the present invention may be implemented in source synchronous links implementing single-ended clock or data strobe signal as well.

As will be described in detail below, in certain aspects of the invention, the data transmitted over source synchronous link 106 is "double pumped." That is, the data signal 120 is transmitted at twice the frequency as the differential data strobe 122. That is, source synchronous transmitter 108 is responsible for the transfer of 2 bits of data over a single data line. That is, transmitter 108 and receiver 110 manage, in a preferred embodiment, 2 bits of data with every data strobe pulse. A source synchronous link implementing the present invention may include any number of data lines in conjunction with the one (single-ended) or two (differential) data strobe line(s). For example, in one implemented embodiment, the present invention is implemented in a source synchronous environment wherein 36 bits are transferred from transmitter 108 and receiver 110. Thus, in embodiments wherein the source synchronous link is double pumped with 2 bits transmitted over each data line, there are 18 data lines and 1 or 2 data strobe lines in communication link 106. It should also be understood, then, that each such transmitter 108 and receiver 110 are replicated 18 times. It should also be noted, however, that the present invention is scalable to any size system to satisfy any communication requirement. For ease of illustration, however, the drawings will depict a single data

slice only.

In the illustrative embodiment, the differential data strobe is a 250MHz clock signal derived from local clock CLK250 116 and the data signal 120 is a 500 MHz data signal derived from local clock CLK500 118. As will be described below, in certain aspects of the invention, the relative clock frequencies are such that the logic level transitions are synchronized. However, the present invention may implement data strobe(s) having a frequency other than 250 and 500 MHz.

The terms “node”, “core”, “logic”, “circuit” and the like should be interpreted broadly when considered in conjunction with the present invention. Such terms embody any and all implementations of the disclosed functions and operations. Further, other terms such as module, unit, system, subsystem and the like should not be construed limiting in any way and are provided to facilitate structural, operational or functional relationships.

### C. Exemplary Data Capture Debug System

Figure 1B is a block diagram of an exemplary debug system in which aspects of the present invention may be implemented. As noted, certain aspects of the present invention are utilized to determine whether source synchronous receiver 110 has properly captured the data transmitted from transmitter 108. The exemplary debug system 150 includes source synchronous transmitter 108 and receiver 110, the details of which are set forth below. In addition, debug system 150 includes data capture debug logic 152 operationally coupled to processing core 102, and data capture storage and analysis logic 154 operationally coupled to processing core 104. In accordance with aspects of the present invention, debug logic 152 controls transmitter 108 to halt differential data strobe 122 when transmitting a predetermined bit pattern 166 to receiver 110. Data capture storage and analysis logic 154 subsequently scans data capture flip-flops (not shown) in source synchronous receiver 110 to retrieve and store captured data 156 for comparison with the transmitted debug pattern 166.

A debug FIFO 162 in processing core 102 stores one or more predetermined debug bit patterns 164A-164N for transmission over communications link 106. Such bit

patterns 164 may be arranged to include specific patterns designed to identify certain capabilities of the implemented source synchronous link. One such bit pattern is chosen as selected debug pattern 166. Data capture debug logic 152 controls multiplexer 170 to input selected debug pattern 166 to data transmit logic 112. Under normal operating  
5 conditions, core data 168 is provided to data transmit logic 112 for transmission.

Data capture debug logic 152 generates one or more data strobe control commands 160 to cause data strobe transmit logic 114 to halt differential data strobe 122. Halting the data strobes transmitted over communication link 106 provides an opportunity for data capture storage and analysis logic 154 to scan the data stored in data capture flip-  
10 flops in receiver 110. This is because the data strobe signals control the data capture flip-flops and, when the data strobe signals are halted, no additional data is written to the data capture flip-flops.

It should be appreciated from the present disclosure that providing a source synchronous transmitter that halts the data strobe allows for the evaluation of the captured data without placing additional components in the functional data path. As  
15 such, this aspect of the present invention does not increase the latency of the transmission and, therefore, does not adversely effect the timing margin of the data signal 120.

## **D. Source Synchronous Link Transmitter 108**

### **1. Differential Data Strobe Transmit Logic 114**

Figure 2A is a functional block diagram of differential data strobe transmit logic 114. Differential data strobe transmit logic 114 generates the differential data strobe 122 comprising data strobe signal DS\_OUT 210 and inverse data strobe signal DSN\_OUT 212 over communication link 106. Differential data strobe transmit logic 114 includes differential data strobe signal generator logic 204 that determines the shape of the  
20 waveform of DS\_OUT 210 and DSN\_OUT 212. Transmit logic 114 also includes strobe stopping logic 202 that controls the signal level states used by signal generator logic 205 to cause DS\_OUT 210 and DSN\_OUT 212 to remain halted in a desired logical state.

Signal generator logic 204 selects alternately between two applied signal levels to

generate DS\_OUT 210 and DSN\_OUT 212. Differential data strobe signal generator 204 receives as inputs four logic level signals, two logic level signals for selection to generate DS\_OUT 210 and two logic level signals for selection to generate DSN\_OUT 212. For DS\_OUT 210, the input logic level signals include VDD\_DS 222 and GND\_DS 224.

5 Similarly, for DSN\_OUT 212, the two input logic level signals are GND\_DSN 226 and VDD\_DSN 228.

As indicated by their names, in normal operations during which the differential data strobe 122 is not halted, input signals VDD\_DS 222 and VDD\_DSN 228 are held consistently in their asserted state while GND\_DS 224 and GND\_DSN 226 are held  
10 consistently in their de-asserted state. Under the control of a 250 MHz clock, signal generator 204 selects alternately VDD\_DS 222 and GND\_DS 224 to generate a 250 MHz data strobe signal DS\_OUT 210. Similarly, signal generator logic 204 selects alternately between VDD\_DSN 228 and GND\_DSN 226 to generate a 250 MHz inverse data strobe signal DSN\_OUT 212. As will be described in detail below, the differential data strobe  
15 signals 210, 212 are generated as single ended bits that are opposite in phase with each other. This insures that the differential data strobe and data signals transmitted through source synchronous link 100 are logically and electrically matched. This, in turn, insures that the injected link noise is experienced common-mode.

As noted, strobe stopping logic 202 provides to differential data strobe signal  
20 generator 204 the logic level signals 222-228 for data strobe signal DS\_OUT 210 and inverse data strobe signal DSN\_OUT 212. In this illustrative embodiment, there are a number of command signals generated by processing core 102 that specify when the differential data strobe is to be halted and, preferably, the state in which the differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 are to be halted.

25 In this embodiment, the data strobe control command signals 160 include a HALT\_STB 216. HALT\_STB 216 indicates whether differential data strobe transmit logic 114 is to operate in a normal operating mode (normal toggling of differential data strobe signals 210, 212) or in a halt data strobe mode of operation (differential data strobe signals 210, 212 held in logical state). In addition, a STOP\_STB\_TRIGGER  
30 signal 214 indicates the precise time the differential data strobe 122 is to be halted. The

state in which the data strobe 210 and the inverse data strobe 212 are halted is determined by the state of another input signal, STOP\_STB\_HIGH 220.

Strobe stopping logic 202 includes primarily two functional elements, differential data strobe control logic 208 and pulse stretch logic 206. Pulse stretch logic 206 generates a data strobe stop signal STOP\_STB 230 that remains in the asserted logical state for the duration in which the differential data strobe 122 is to be halted. The STOP\_STB 230 signal is used by differential data strobe control logic 208 as described below. Thus, when STOP\_STB 230 is asserted, differential data strobe 122 is halted, and when STOP\_STB 230 is de-asserted, differential data strobe 122 is to transmit normally; that is, as 1 or 2 a pulsed signals. It should be understood that there are a myriad of other techniques that one can implement to communicate such information.

Pulse stretch logic 206 receives as inputs the strobe halt mode signal HALT\_STB 216 and the halting trigger STOP\_STB\_TRIGGER 214. Also, an active low reset signal RESET\_LOW 218 is provided to pulse stretch logic 206. In accordance with certain aspects of the invention, the STOP\_STB\_TRIGGER 214 and HALT\_STB 216 signals are registered at a first clock frequency, here, 250MHz, prior to being provided to pulse stretch logic 206.

When the differential data strobe 122 is to be halted, HALT\_STB 216 is asserted. RESET\_LOW 218 is an active low signal and, therefore, is asserted in non-reset conditions. Thus, when the stop trigger signal STOP\_STB\_TRIGGER 214 is received while transmit logic 114 is in the halt data strobe mode of operation (HALT\_STB 216 is asserted) and transmit logic 114 is not reset (RESET\_LOW 218 is asserted), the stop strobe signal STOP\_STB 230 is asserted. STOP\_STB 230 remains asserted until the device is reset or HALT\_STB 216 changes logical state indicating that the differential data should no longer be halted.

Differential data strobe control logic 208 sets the logic levels that are used to generate the transmitted differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 in response to STOP\_STB 230 and STOP\_DS\_HIGH 220. In this illustrative embodiment, the differential data strobe 122 may be halted with the data strobe signal DS\_OUT 210 asserted and the inverted data strobe signal DSN\_OUT 212 de-asserted, or

with DS\_OUT 210 de-asserted and DSN\_OUT 212 asserted. Differential data strobe control logic 208 makes this determination based on the state of the control signal STOP\_DS\_HIGH 220 when the stop strobe signal STOP\_STB 230 indicates that the differential data strobe is to be halted. The data strobe and inverse data strobe signals are to be halted in the specified state for the period of time in which stop strobe signal 230 is asserted.

Differential data strobe control logic 208 controls the four logic level signals provided to level select logic 204. Of the four signals, two provide logical high (VDD\_DS 222) and low (GND\_DS 224) signals for DS\_OUT 210 while the other two provide logical high (VDD\_DSN 228) and low (GND\_DSN 226) signals for DSN\_OUT 212. As noted, under normal operating conditions, these four signals remain at their respective logical high and low states indefinitely. This enables level select logic 204 to alternatively select VDD\_DS 222 or GND\_DS 224 to drive DS\_OUT 210, and to select either GND\_DSN 226 or VDD\_DSN 228 to drive DSN\_OUT 212. This generates, as noted, two individual signals that toggle out of phase with each other at 250MHz.

In accordance with aspects of the present invention, the differential data strobe 122 is halted by virtue of control logic 208 changing the logical state of one or more of the logic level signals 222-228 provided to level select logic 204. As will be described in detail below, when the differential data strobe 122 is to be halted with DS\_OUT 210 asserted, then the logical state of GND\_DS 224 is changed from a de-asserted state to an asserted state so that when signal generator 204 switches from VDD\_DS 222 to GND\_DS 224 to drive DS\_OUT 210, the same asserted logical state is provided continually to signal generator 204. As a result, DS\_OUT 210 is continually in the asserted state. Similarly, should the differential data strobe 12 be halted with DS\_OUT 210 in the de-asserted state, then data strobe control logic 208 changes the logical state of VDD\_DS 222 from its asserted state to a de-asserted state so that when signal generator 204 switches from VDD\_DS 222 to GND\_DS 224, the same low logical state is provided to signal generator 204. This results in DS\_OUT 210 having a continuous de-asserted logical state as it toggles between VDD\_DS 222 and GND\_DS 224. This same approach is implemented to control the inverse data strobe signal DSN\_OUT 212 by adjusting the



logical states of VDD\_DSN 228 and GND\_DSN 226.

It should be noted that this approach to halting the differential data strobe is exemplary only and, in particular, is provided to accommodate the interface requirements with differential data strobe signal generator 204. By controlling the logical level signals provided to differential data strobe signal generator 204, this embodiment of the invention places all logic for halting the differential data strobe 122 in the strobe stopping logic 202, enabling the signal generator 204 to remain unchanged. Those of ordinary skill in the art will appreciate that other implementations would be possible without deviating from the scope of the present invention.

As noted, while differential data strobe signals 210, 212 are halted by strobe stopping logic 202, no additional data can be clocked into the source synchronous receiver 110. The data received immediately before the halting of the differential data strobe can then be scanned from receiver 110 for analysis.

#### **a. Data and Data Strobe Signal Relationship**

Also illustrated in Figure 2A is a functional representation of data transmit logic 112. As will be described in greater detail below, data transmit logic 112 implements a logic structure that is identical to that implemented by differential data strobe signal generator 204 to insure the data signal 120 and differential data strobe signal 122 have substantially identical experiences in terms of interference and noise as they are generated by source synchronous link transmitter 108.

To further insure such similar experiences, the data transmitted over source synchronous link 116 is “double pumped.” That is, data is transmitted over the data link at twice the frequency as the differential data strobe 122. In the illustrative embodiment, the differential data strobe has a frequency of 250MHz. Thus, in this embodiment, DATA\_OUT 234 operates at 500 MHz. A timing diagram illustrating the relationship between these signals is provided in Figure 2B.

Referring now to Figure 2B the 250MHz clock CLK250 116 and the 500 MHz clock CLK500 118 are depicted at the top of the figure. Below these two exemplary

waveforms are the two data core signals received by data transmit logic 112 from processing core 102, DATA0\_CORE 236 and DATA1\_CORE 232. Each such signal provides two bits of data in this example. Bits D0 and D2 are provided at time periods T1 and T2 on DATA0\_CORE 236 and bits D1 and D3 are provided at time periods T1 and T2 on DATA1\_CORE 232.

As will be described in detail below, data transmit logic 112 transmits the received data on a DATA\_OUT signal 234 at twice the frequency of the differential data strobe of 250MHz, or 500 MHz. This is illustrated in Figure 2B with data bits D0 and D1 being transmitted during time period T2 and data bits D2 and D3 being transmitted during time period T3.

The differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 are depicted immediately below DATA\_OUT 234. Comparing these three signals illustrates the alignment of logic level transitions. That is, each occurrence of a signal transition in the differential data strobe signals 210, 212, occurs at the same time and at the same frequency as the signal transitions of the data signal 234. As noted, this insures that the data and data strobe lines of communication link 106 experience the same electrical modes. This contributes to the electrical matching of the data and data strobes, thereby maximizing link margins.

At the bottom of Figure 2B another data signal is illustrated, also referred to as DATA\_OUT 234. This latter waveform of DATA\_OUT 234 illustrates the phase shifting imparted on DATA\_OUT 234 when it is received at source synchronous receiver 110. The captured data signal 234 is shifted relative to the differential data strobe signals 210, 212 by one 500 MHz clock period, placing the rising and falling edges of DS\_OUT 210 and DSN\_OUT 212 in the center of the data signal DATA\_OUT 234. As will be described in detail below, the data signal DATA\_OUT 234 is latched into source synchronous receiver 110 at the rising edges of DS\_OUT 210 and DSN\_OUT 212. By shifting the relative phase of the data and data strobe signals to center the differential data strobe edges in the data eye insures the data signal DATA\_OUT 234 is stable before it is latched into source synchronous receiver 110. In a preferred embodiment, this is achieved by adding extra delay into the media that carries the differential data strobe

signals. In a preferred embodiment, extra trace is added to the printed circuit board.

**b. Data Strobe Halt Command and Data Strobe Signal Relationship**

Figure 3 is a timing diagram illustrating the relationship between the control signals received from processing core 102 and the resulting state of the differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 in accordance with one aspect of the present invention. In Figure 3 the reference numerals for the signals/signal lines are provided in a parenthetical after the signal name to facilitate correlation with the embodiment of differential data strobe transmit logic 114 illustrated in Figure 2A. It should be noted that there is no implied relationship between the time periods T<sub>n</sub> illustrated in Figure 3 and the time periods illustrated in other timing diagrams provided herein unless expressly stated. Also, the labeled time periods represent cycles of the 250 MHz clock CLK250 116.

As noted, there are three signals that are provided by processing core 102 to control the halting of the differential data strobe 122 and the state of the halted differential data strobe signals in this embodiment of the invention. These control signals include HALT\_STB 216, STOP\_DS\_HIGH 220 and STOP\_STB\_TRIGGER 214. In this example, HALT\_STB 216 transitions from a low logical state to a high logical state during time interval T1 indicating that transmit logic 114 is to halt the differential data strobe upon receipt of a stop strobe trigger signal STOP\_STB\_TRIGGER 214. In this example, a STOP\_DS\_HIGH 220 is also asserted during time period T1 indicating that DS\_OUT 210 is to be halted in the asserted logical state. In response, transmit logic 114 enters a state during which it waits for the receipt of trigger signal STOP\_STB\_TRIGGER 214 to halt the differential data strobe signals DS\_OUT 210 and DSN\_OUT 212.

In this example, STOP\_STB\_TRIGGER 214 is received at the same time as the other two control signals, that is, during time period T1, although this need not be the case. Control signals 216, 220 and 214 are registered in the 250MHz clock domain. On the first rising edge of the 250 MHz clock CLK250 116, STOP\_STB\_TRIGGER 214 is latched into strobe stopping logic 202. This is described in greater detail below. The 250

MHz clock cycle after STOP\_STB\_TRIGGER 214 is latched, strobe stopping logic 202 processes the signal. As indicated at the top of Figure 3, there is an approximate 4ns delay. At the following rising edge of CLK250, time period T3, the differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 are halted in the state specified by

5 STOP\_DS\_HIGH 220.

The differential data strobe signals 210, 212 remain in their halted states until HALT\_STB 216 transitions to a de-asserted state indicating that differential data strobe transmit logic 114 to cease operating in the halt data strobe mode of operation and return to the normal modes of operation. HALT\_STB 216 transitions to a logical low state

10 during time period T5 which is latched at the next rising clock edge, time period T6. After a one cycle delay (time period T6), the differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 return to normal operations at the next falling edge during time period T7.

It should be appreciated to those of ordinary skill in the art that the same information

15 can be communicated from processing core 102 to source synchronous transmitter 108 using more or less command signals. The use of such variations is considered to be within the scope of the present invention.

### c. Pulse Stretch Logic 206

As noted, pulse stretch logic 206 generates the data strobe stop signal STOP\_STB

20 230 that is used by control logic 208 as described herein. Pulse stretch logic 206 receives as inputs the strobe halt mode signal HALT\_STB 216 and the halting trigger STOP\_STB\_TRIGGER 214. Also, active low reset signal RESET\_LOW 216 is also provided to pulse stretch logic 206.

Preferably, STOP\_STB\_TRIGGER 214 and HALT\_STB 216 are AND'ed with

25 RESET\_LOW 218 prior to being received by pulse stretch logic 206 to prevent the two control signals from being asserted during a system reset condition. Both signals are latched into a flip-flop using a 250MHz clock signal prior to being provided to pulse stretch logic 206.

Referring now to the exemplary embodiment of pulse stretch logic 206 illustrated in Figure 4, there are two NOR gates 402 and 404 and a flip-flop 406 clocked by the 500 MHz clock signal 118. STOP\_STB\_TRIGGER 214 and a signal indicating whether the stop strobe trigger STOP\_STB\_TRIGGER 214 was asserted previously are provided as inputs to NOR gate 402. STOP\_STB\_PREV 414 is input into NOR gate 402. The output of NOR gate 402 is INT\_NODE\_A 408. The operation of NOR gate 402 is provided below. NOR gate 404 has 3 inputs: INT\_NODE\_A 408, HALT\_STB\_NOT 410 and RESET\_LOW\_NOT 412. The output of NOR gate 404 is STOP\_STB 230. This signal is latched into flip-flop 406 using the 500 MHz clock CLK500 118. This signal is also provided to differential data strobe control logic 208 as the signal controlling the invocation and duration of the halted differential data strobe 122.

When the differential data strobe 122 is to be halted, HALT\_STB 216 is asserted. Inverter 416 inverts HALT\_STB 216. The inverted signal is referred to as HALT\_STB\_NOT 410. Thus, HALT\_STB\_NOT 410 is de-asserted during the halt data strobe mode of operation and is asserted during the normal operational mode. Similarly, RESET\_LOW 218 is an active low signal and, therefore, is asserted in non-reset conditions. Inverter 418 inverts RESET\_LOW 218. The inverted signal is referred to as RESET\_LOW\_NOT 412. RESET\_LOW\_NOT 412 remains de-asserted during this example. As such, the output of NOR gate 408, STOP\_STB 230, will have the same logical state as the third input, INT\_NODE\_A 408 until the device is reset or the data strobes are no longer halted.

With regard to NOR gate 402, if either input, STOP\_STB\_TRIGGER 214 or STOP\_STB\_PREV 414 is asserted, NOR gate 402 de-asserts INT\_NODE\_A 408, causing STOP\_STB 230 to be asserted. STOP\_STB 230 is clocked into flip-flop 406 at the next occurring rising edge of the 500 MHz clock CLK500 118 and returned to NOR gate 402. This will thereafter cause the output of NOR gate 402 INT\_NODE\_A 408 to remain asserted. Thus, when the stop trigger signal STOP\_STB\_TRIGGER 214 is received while transmit logic 114 is in halt data strobe mode of operation (HALT\_STB 216 is asserted) and transmit logic 114 is not reset (RESET\_LOW 218 is asserted), the stop strobe signal STOP\_STB 230 is asserted. STOP\_STB 230 remains asserted until the

device is reset or HALT\_STB 216 changes state indicating that the differential data strobe is to no longer be halted.

Figure 5 is a timing diagram illustrating the operation of pulse stretch circuit 206 when the strobe stopping logic 202 receives instructions to enter the strobe halting mode of operation. As with the other timing diagrams, in Figure 5 the reference numerals for the signals/signal lines are provided in a parenthetical after the signal name to facilitate correlation with the embodiment of pulse stretch logic 206 illustrated in Figure 4. Also, the time periods illustrated in Figure 5 have no relationship with other timing diagrams illustrated herein unless expressly stated.

In time period T1 HALT\_STB 216 is asserted invoking the halt data strobe mode of operation and placing pulse stretch circuit 206 in a waiting state. When STOP\_STB\_TRIGGER 214 is asserted at time T2, STOP\_STB 230 is asserted. This relationship is illustrated in Figure 5 by arrow 502. As shown, STOP\_STB\_TRIGGER 214 is asserted for less than one clock 250 cycle. However, as noted, STOP\_STB 230 remains in an asserted state until HALT\_STB 216 is de-asserted at time period T6. This relationship is illustrated in Figure 5 by arrow 504.

As noted, STOP\_STB 230 is latched at 500 MHz by flip-flop 406. This is illustrated in Figure 5 as the rising edge of signal 408 occurring at the next rising edge of CLK500 118 after the transition of STOP\_STB 230, as illustrated by arrow 506.

It should be understood that pulse stretch logic 206 may be implemented in numerous other configurations and with many other circuit components. It should also be understood that the logic elements illustrated in Figure 4 are dictated by the need to provide a stop strobe signal 230 in response to the occurrence of the triggering event until instructed otherwise. Here, the condition that ceases the end of halting of the differential data strobe 122 is the end of the halt data strobe mode of operation, as represented by the de-assertion of the signal HALT\_STB 216. Other conditions represented by other signals may be utilized. Furthermore, NOR gate 402 and flip-flop 406 are provided to maintain STOP\_STB 230 in an asserted state after trigger signal 214 is de-asserted. Such elements are unnecessary in embodiments wherein trigger signal 214 remains asserted for the period of time during which the data strobe is to be halted.

**d. Differential Data Strobe Control Logic 208**

Differential data strobe control logic 208 sets the logic levels that are used to generate the transmitted differential data strobe 122 signals DS\_OUT 210 and DSN\_OUT 212. As noted, the differential data strobe 122 may be halted with the data strobe signal DS\_OUT 210 asserted and the inverted data strobe signal DSN\_OUT 212 de-asserted, or with DS\_OUT 210 de-asserted and DSN\_OUT 212 asserted.

Differential data strobe control logic 208 makes this determination based on the state of the control signal STOP\_DS\_HIGH 220. When STOP\_DS\_HIGH 220 is asserted, the differential data strobe 122 is halted with DS\_OUT 210 in the asserted state and DSN\_OUT 212 in the de-asserted state. When STOP\_DS\_HIGH 220 is de-asserted, the differential data strobe 122 is halted with DS\_OUT 210 in the de-asserted state and DSN\_OUT 212 in the asserted state. However, as noted, control logic 208 performs these operations only when the stop strobe signal STOP\_STB 230 received from pulse stretch circuit 206 is asserted.

Differential data strobe control logic 208 controls the four logic level signals 222-228 provided to level select logic 204. Of the four logic level signals, two provide logical high (VDD\_DS 222) and low (GND\_DS 224) logic level signals for DS\_OUT 210 while the other two provide logical high (VDD\_DSN 228) and low (GND\_DSN 226) logic level signals for DSN\_OUT 212. Under normal operating conditions, these four signals remain at their respective logical high and low states indefinitely. This enables signal generator 204 to alternately select VDD\_DS 222 or GND\_DS 224 to drive DS\_OUT 210, and to alternately select either GND\_DSN 226 or VDD\_DSN 228 to drive DSN\_OUT 212. Thus, DS\_OUT 210 and DSN\_OUT 212 are simply two individually controlled signals that are out of phase with each other.

In this embodiment of the present invention, the differential data strobe 122 is halted by virtue of control logic 208 changing the logical state of one or more of the logic level signals 222-228 provided to signal generator 204. As noted, when the differential data strobe 122 is to be halted with DS\_OUT 210 asserted, then the logical state of GND\_DS 224 is changed from a de-asserted state to an asserted state. When signal generator 204 switches from VDD\_DS 222 to GND\_DS 224 to transmit as DS\_OUT 210, it thereafter

receives the same asserted logical state. As a result, DS\_OUT 210 is continually in that same asserted state. Similarly, should the differential data strobe 122 be halted with DS\_OUT 210 in the de-asserted state, then data strobe control logic 208 changes the logical state of VDD\_DS 222 from its asserted state to a de-asserted state. When signal generator 204 switches from VDD\_DS 222 to GND\_DS 224, the same low logical level is thereafter received, resulting in DS\_OUT signal 210 having a continuous de-asserted logical state as it toggles between VDD\_DS 222 and GND\_DS 224. This same approach is implemented to control the inverse data strobe signal DSN\_OUT 212 by adjusting the logical states of VDD\_DSN 228 and GND\_DSN 226.

Turning now to the logic elements illustrated in Figure 6, control logic 208 includes four gates each generating one of the four logic level signals 22-228 as its output. Specifically, VDD\_DS 222 is the output of a NAND gate 602 having the strobe stop signal STOP\_STB 230 and the inverse of the data strobe halt high signal STOP\_DS\_HIGH\_NOT 613 provided as its inputs. GND\_DS 224 is the output of a NOR gate 604 having the inverse of the stop strobe signal, STOP\_STB\_NOT 616, and STOP\_DS\_HIGH\_NOT 613 provided as its inputs. GND\_DSN 226 is the output of a NOR gate 606 having STOP\_STB\_NOT 616 and STOP\_DS\_HIGH 220 provided as its inputs. VDD\_DSN 228 is the output of a NAND gate 608 having STOP\_STB 230 and STOP\_DS\_HIGH 220 as provided at its input ports.

With regard to NAND gate 602, when the differential data strobe 122 is to be halted, as indicated by the assertion of STOP\_STB 230, the output of NAND gate 602, VDD\_DS 222, will then be the inverse of STOP\_DS\_HIGH\_NOT 614, or the same state as STOP\_DS\_HIGH 220. Thus, when the data strobe signal DS\_OUT 210 is to be in the asserted state when halted (STOP\_DS\_HIGH 220 is logical high), then VDD\_DS 222 is set to its asserted state. When the data strobe 122 is to be in the de-asserted state when halted (STOP\_DS\_HIGH 220 is logical low), then VDD\_DS 222 is set to its de-asserted state.

With regard to NOR gate 604, when the differential data strobe is to be halted, as indicated by the asserted state of STOP\_STB 230, the inverse signal, STOP\_STB\_NOT 616 is applied to one input of NOR gate 604. The output of NOR gate 604, GND\_DS



224, is then the inverse of the other input, STOP\_DS\_HIGH\_NOT 614 and, therefore, has the same state as STOP\_DS\_HIGH 220. Thus, if the data strobe signal DS\_OUT 210 is to be in the asserted state when halted, then GND\_DS 224 is set to its asserted state. When the data strobe DS\_OUT 210 is to be halted in the de-asserted state, then  
5 GND\_DS 224 is set to its de-asserted state. Thus, when the differential data strobe 122 is to be halted, both, VDD\_DS 222 and GND\_DS 224 are set to the desired state in which the data strobe signal DS\_OUT 210 is to be halted.

With regard to NOR gate 606, when the differential data strobe is to be halted as indicated by the asserted state of STOP\_STB 230, the inverse signal, STOP\_STB\_NOT 616 is applied to one input of NOR gate 606. The output of NOR gate 606, GND\_DSN  
10 226, will then have a logical state that is the inverse of STOP\_DS\_HIGH 220. Thus, if the inverse data strobe signal DSN\_OUT 212 is to be in the de-asserted state when halted (STOP\_DS\_HIGH 220 is de-asserted), then GND\_DSN 226 is set to its de-asserted state. Conversely, when the differential data strobe 122 is to be halted with DSN\_OUT 212  
15 asserted, then NOR gate 606 asserts GND\_DSN 226.

Finally, with regard to NAND gate 608, when the differential data strobe 122 is to be halted with DS\_OUT 210 asserted, as indicated by STOP\_STB 230 being asserted, then the output of NAND gate 602, VDD\_DSN 228, will be the inverse of STOP\_DS\_HIGH 220. Thus, when DSN\_OUT 212 is to be in the de-asserted state when halted,  
20 VDD\_DSN 228 is set to its de-asserted state. Conversely, when DSN\_OUT 212 is to be in the asserted state when halted, VDD\_DSN 228 is set to its asserted state. Thus, when the differential data strobe 122 is to be halted both, VDD\_DSN 228 and GND\_DSN 226 are set to the inverse of the state of STOP\_DS\_HIGH 220; that is, the opposite of the specified state of the data strobe signal DS\_OUT 210.

Figure 7 is a timing diagram illustrating the relationship between the signals related to differential data strobe control logic 208 when the strobe stopping logic 202 receives instructions to enter the halt data strobe mode of operation. In Figure 7 the reference numerals for the signals/signal lines are provided in a parenthetical after the signal name to facilitate correlation with differential data strobe control logic 208 illustrated in Figure  
25 6. Also, the time periods illustrated in Figure 7 have no relationship with other timing  
30

diagrams illustrated herein unless expressly stated.

In the example sequence illustrated in Figure 7, STOP\_DS\_HIGH signal 220 is asserted at time period T1. This indicates that when the differential data strobe is halted, that the data strobe signal DS\_OUT 210 should be halted in the high logical state while the data strobe not signal DSN\_OUT 212 should be halted in the low logical state. During time period T1, VDD\_DS 222 is asserted, GND\_DS 224 is de-asserted, VDD\_DSN 228 is de-asserted and GND\_DS 228 is asserted (that is, in normal mode).

Upon receipt of the stop strobe signal STOP\_STB 230, certain of the level signals 222-228 are altered to accommodate the specified logic level for DS\_OUT 210 and DSN\_OUT 212. Since STOP\_STB\_HIGH 220 is asserted in this example, GND\_DS 224 transitions from a de-asserted to an asserted state in time period T2. This is illustrated by arrows 702 and 704 in Figure 7. GND\_DS 224 remains in this state until STOP\_STB 230 is de-asserted. Thus, for time periods T2-T4, VDD\_DS 222 and GND\_DS 224 have the same asserted state. Thus, as level select logic 208 alternates between VDD\_DS 222 and GND\_DS 224 to drive DS\_OUT 210, the same logic level is provided to control logic 208 during time periods T2-T4. When the differential data strobe is to no longer be halted, STOP\_STB 230 is de-asserted, causing GND\_DS 224 to return to its normal de-asserted state. This is illustrated by arrow 706 in Figure 7.

Similarly, GND\_DSN 226 transitions from a high state to a low state in time period T2 and remains in the de-asserted state until time period T4. See arrows 702-706 in Figure 7. VDD\_DSN 228 is not altered and remains in a de-asserted state. Thus, for time periods T2-T4 VDD\_DSN 228 and GND\_DSN 226 have the same de-asserted state. Thus, as level select logic 208 alternates between VDD\_DSN 228 and GND\_DSN 226 to drive DSN\_OUT 212, the same logic level is provided to control logic 208 during time periods T2-T4.

### e. Differential Data Strobe Signal Generator Logic

Figure 8 is an architectural block diagram of differential data strobe signal generator 204. Signal generator 204 selects alternately between two applied signal levels to generate DS\_OUT 210 and DSN\_OUT 212. As noted, differential data strobe level select logic 204 receives as inputs the four logic level signals VDD\_DS 222, GND\_DS 224, GND\_DSN 226 and VDD\_DSN 228. Either VDD\_DS 222 or GND\_DS 224 is selected as DS\_OUT 210. Similarly, either GND\_DSN 226 or VDD\_DSN 228 is selected as DSN\_OUT 212.

During normal operations, these input signals are consistently held in the asserted (VDD\_DS 222 and VDD\_DSN 228) and de-asserted (GND\_DS 224 and GND\_DSN 226) states. During normal operations the data strobes are 250 MHz pulses with DS\_OUT being the inverse of DSN\_OUT. These pulses are generated by selecting VDD\_DS 222 for the first half of a 250MHz cycle and GND\_DS 224 for the second half. Similarly, DSN\_OUT 212 selects GND\_DSN 226 for half of a 250 MHz cycle and VDD\_DSN 228 for the other half cycle.

Referring now to Figure 8, in accordance with certain aspects of the present invention, redundant components are implemented in signal generator 204 to select the logic level for DS\_OUT 210 and DSN\_OUT 212. Specifically, a series of transparent latches and D flip-flops, described below, are provided to latch the level signals VDD and GND for each data strobe signal DS\_OUT and DSN\_OUT. Each such latch imposes an additional delay to the signal depending on whether the latches and flip-flops are responsive to the rising or falling edges of the 250 MHz clock CLK250 116 or 500 MHz clock CLK500 118.

The input level signals VDD\_DS 222 and GND\_DS 224 are passed through transparent latches 802, 804, respectively when the inverse of the 250 MHz clock signal CLK250\_NOT 826 is asserted. The nomenclature used for the latched signals refer to the latch rate and include an "LA" to indicate it is the latched signal. Thus, the signal output from latch 802 is referred to as VDD\_DS\_250\_LA 828. GND\_DS\_250\_LA 830 is then provided to transparent latch 810 which passes the signal through when the 500 MHz clock is asserted. The resulting signal, GND\_DS\_500\_LA 832 is provided as one

of two inputs to a multiplexer 816. The other input to multiplexer 816 is VDD\_DS\_250\_828. MUX\_SELECT signal 834 selects which of the two inputs, VDD\_DS\_250\_LA 828 or GND\_DS\_500\_LA 832 is to be presented as DS\_SELECT 842 at any given time. Multiplexer 816 is controlled by MUX\_SELECT signal 834.

5 MUX\_SELECT 834 is a 250 MHz pulse synchronized with CLK500 116 due to the inverter 824 inverting CLK250\_NOT 826. The 250 MHz clock is latched into flip-flop 812 using the falling edge of the 500 MHz clock to generate MUX\_SELECT 834. MUX\_SELECT 834 rises on the falling edge of CLK500 118, driving multiplexer 816 with a 250 MHz pulse that is shifted by half of a 500 MHz cycle.

10 The output of multiplexer 816, DS\_SELECT 842, follows GND\_DS\_500\_LA 832 when MUX\_SELECT 834 is asserted and follows VDD\_DS\_250\_LA 828 when MUX\_SELECT 834 is de-asserted. The output of multiplexer 816, DS\_SELECT 842, is latched into flip-flop 820 at 500 MHz to generate DS\_OUT 210. Thus, a change in state of DS\_SELECT 842 is detected at the next rising edge of the 500 MHz clock.

15 Similar logic is provided for selecting the level of DSN\_OUT 212. Referring again to Figure 8, the input level signals 226, 228 are received by signal generator 204 by transparent latches 806, 808, respectively. Latches 806, 808 are controlled by an inverse 250 MHz clock signal CLK250\_NOT 826. GND\_DSN 226 is passed through transparent latch 806 when CLK350\_NOT is asserted, with the latched signal referred to as  
20 GND\_DSN\_250\_LA 836. VDD\_DSN\_250\_LA 838 is then provided to transparent latch 814 which operates at 500 MHz. The resulting signal VDD\_DSN\_500\_LA 840 is provided as one of two inputs to a multiplexer 818. The other input is GND\_DSN\_250\_LA 836.

MUX\_SELECT signal 834 selects which of the two inputs, GND\_DSN\_250\_LA  
25 836 or VDD\_DSN\_500\_LA 840 are to be presented as DSN\_SELECT 844. As noted, MUX\_SELECT 834 is a 250 MHz pulse that continually alternates between the two inputs, rising on the falling edge of CLK500 118. The output of multiplexer 818, DSN\_SELECT 844, follows GND\_DSN\_250\_LA 836 when MUX\_SELECT 834 is de-asserted and follows VDD\_DSN\_500\_LA 840 when MUX\_SELECT 834 is asserted.  
30 MUX\_SELECT 834 drives multiplexer 818 with a 250 MHz pulse that is shifted by half

of a 500 MHz cycle. The output of multiplexer 818, DSN\_SELECT 844 is latched at 500 MHz by flip-flop latch 822 to generate DSN\_OUT 212. Thus, a change in state of DSN\_SELECT 844 is detected at the next rising edge of the 500 MHz clock.

Thus, as shown in Figure 8 and as described above, in certain aspects of the present invention, signal generator 204 includes redundant components to generate DS\_OUT 210 and DSN\_OUT 212. In addition to the same components in the same configuration, the components utilize the same system clocks. By providing the same physical and electrical configuration of components, these two signals experience injected link noise common-mode.

Figure 9 is a diagram illustrating the timing relationships between the signals that appear in Figure 8. In this timing diagram there are six time periods. The four input logic level signals are shown at the top of Figure 9. During the first time period (and before) they were at levels associated with the normal mode of operation. That is, VDD\_DS 222 and VDD\_DSN 228 were in the asserted state and GND\_DS 224 and GND\_DSN 226 were in the de-asserted state.

In this exemplary sequence of waveforms, from time period T2 through time period T4 transmitter 108 is in the halt data strobe mode of operation. The specified logic levels of signals 222-228 is such that DS\_OUT 210 will be halted in the asserted state while DSN\_OUT 212 will be halted in the de-asserted state. To achieve this, GND\_DS 224 transitions from a de-asserted to an asserted state for these time periods as shown in Figure 9. As a result, both, VDD\_DS 222 and GND\_DS 224 are in their asserted states for the relevant time periods. As noted, level select logic 204 alternately selects VDD\_DS 222 and GND\_DS 224 to transmit as DS\_SELECT 842. With both such signals in the asserted state the selection of either will cause DS\_SELECT 832 to be continually in the asserted state; that is, halted in the asserted state.

Conversely, VDD\_DSN 228 transitions from an asserted state to a de-asserted state for time periods T2-T4. Thus, during the relevant time period both GND\_DSN 226 and VDD\_DSN 228 are in the de-asserted state. As noted, level select logic 204 alternately selects GND\_DSN 226 and VDD\_DSN 228 to transmit as DSN\_SELECT 844. With both such signals in the de-asserted state during time periods T2 through T4, the

selection of either will cause DSN\_SELECT 844 to be continually in the de-asserted state; that is, halted in the de-asserted state.

The corresponding latched signals 828, 830, 836, 838 and 840 are also illustrated in Figure 900. As shown, the signal level signals 222-228 are passed through their  
5 respective transparent latch when CLK250 116 is de-asserted due to the use of the inverse clock signal CLK250\_NOT 826 to provide the clock input to latches 802-808. Since GND\_DS 224 and VDD\_DSN 228 transition at a rising edge of CLK250 116, there is a half cycle delay between the latched signals 828, 830, 836 and 838 and the signals 222-228. One example of this is illustrated by arrow 912 showing the  
10 relationship between the rising edge of GND\_DS 224 and the subsequent rising edge of GND\_DS\_250\_LA 830.

Below the latch signals in Figure 9 is MUX\_SELECT signal 834. As noted, MUX\_SELECT is a 250 MHz pulse that alternately selects continuously between the two inputs of the multiplexers 816 and 818. MUX\_SELECT 834 rises on the falling edge of  
15 CLK500 118 and drives multiplexer 816 with a 250 MHz pulse that is shifted by half of a 500 MHz cycle.

Turning now to DS\_SELECT 842, when MUX\_SELECT 834 is asserted, DS\_SELECT 842 is set equal to GND\_DS\_500\_LA 832 and when MUX\_SELECT 834 is de-asserted, DS\_SELECT 842 is set equal to VDD\_DS\_250\_LA 828. Thus,  
20 DS\_SELECT 842 transitions to and maintains an asserted state in response to GND\_DS\_500\_LA 832 transitioning at the rising edge of CLK500 118 during time period T2. This is illustrated by arrow 902 in Figure 9. DS\_SELECT 842 remains in the asserted state until GND\_DS\_500\_LA 832 is de-asserted, as shown by arrow 904 in Figure 9. A similar relationship exists between DSN\_SELECT 844 and  
25 GND\_DSN\_250\_LA 836 and VDD\_DSN\_500\_LA 840. This is illustrated by arrows 906 and 908 in Figure 9.

As noted, DS\_SELECT 842 is latched by flip-flop 820 using the rising edge of CLK500 118. Thus, DS\_OUT 210 transitions to the state of DS\_SELECT 842 at the next rising edge of CLK500 118. As a result, in this example, DS\_OUT 210 is shifted  
30 from DS\_SELECT 842 by a 500 MHz cycle. This is illustrated by arrow 910 in Figure 9.

## 2. Data Transmit Logic 112

Figure 11 is an architectural circuit diagram of one embodiment of data transmit logic 112. As noted, data transmit logic 112 receives data from processing core 102 at 250 MHz and transmits that data onto communication link 106 at a clock rate of 500 MHz. As will be described in detail below, the data signal 120 is preferably driven at twice the period of the data strobe signals. This causes the data strobe signal 122 and data signal 120 to transition logical states at the same time and at the same frequency, insuring maximally similar electrical modes on the communication link, further maximizing link margin.

In accordance with another aspect of the invention, DATA\_OUT 234 and differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 are processed through the same logical and physical components in source synchronous transmitter 108. Thus, the configuration of data transmit logic 112 illustrated in Figure 11 is the same as one half of the circuit configuration of data strobe signal generator 204 illustrated in Figure 8. As noted, this insures injected link noise is experienced by both, DATA\_OUT 234 and DS\_OUT 210 and DSN\_OUT 212.

Referring to Figure 8, recall that differential data strobe signal generator 204 generates both differential data strobe signals, DS\_OUT 210 and DSN\_OUT 212. The top portion of Figure 8 is directed to generating DS\_OUT 210 while the bottom half is directed towards generating DSN\_OUT 212. Flip-flop 812 is shared by both portions of circuit 204.

Referring now to Figure 11, data transmit logic 112 will now be described. A series of transparent latches and D flip-flops are provided to latch the two data signals DATA0\_CORE 236 and DATA1\_CORE 232 for data signal DATA\_OUT 234. Each such latch imposes an additional delay to the signal depending on whether the latches and flip-flops are responsive to the rising or falling edges of the 250 MHz clock CLK250 116 or 500 MHz clock CLK500 118.

The data signals DATA0\_CORE 236 and DATA1\_CORE 232 are latched into transparent latches 1102, 1104, respectively, using the inverse of the 250 MHz clock signal CLK250\_NOT 826. The signal output from transparent latch 1102 is D0\_250\_LA

1122. Similarly, the signal output from transparent latch 1104 is D1\_250\_LA 1124.

D1\_250\_LA 1124 is input to transparent latch 1106 which latches the signal using the rising edge of the 500 MHz clock CLK500 118. The resulting signal, D1\_500\_LA 1126 is provided as one of two inputs of a multiplexer 1114. The other input to  
5 multiplexer 1114 is D0\_250\_LA 1122. DATA\_MUX\_SELECT signal 1120 selects which of the two inputs is to be presented as DATA\_SELECT 1128 at any given time. Multiplexer 1114 is controlled by DATA\_MUX\_SELECT signal 1120.

DATA\_MUX\_SELECT signal 1120 is a 250 MHz pulse synchronized with CLK250 116 due to the inverter 1112 inverting CLK250\_NOT 826. The 250 MHz clock is  
10 latched into flip-flop 1108 using the falling edge of the 500 MHz clock CLK500 118 due to inverter 1116. DATA\_MUX\_SELECT 1120 rises on the falling edge of CLK500 118, driving multiplexer 1114 with a 250 MHz pulse that is shifted by half of a 500 MHz cycle from CLK250 116.

The output of multiplexer 1128, DATA\_SELECT 1128, outputs D1\_500\_LA 1126  
15 when DATA\_MUX\_SELECT 1120 is asserted, outputs D0\_250\_LA 1122 when DATA\_MUX\_SELECT 1120 is de-asserted. The output of multiplexer 1114, DATA\_SELECT 1128, is latched into flip-flop 1110 at 500 MHz to generate DATA\_OUT 234. Thus, a change in state of DATA\_SELECT 1128 is detected at the next rising edge of the 500 MHz clock CLK500 118.

20 As noted, data transmit logic 112 is identical to each of the two portions of differential data strobe signal generator 204 that transmit DS\_OUT 210 and DSN\_OUT 212. For example, in one embodiment, latches 802, 804 and 810 are identical to latches 1102, 1104 and 1106, flip-flops 812 and 820 are identical to 1108 and 1110, and multiplexer 816 is identical to multiplexer 1114. In addition the components are  
25 arranged in the same configuration and utilize the same system clocks 116 and 118.

The relationship between the signals illustrated in Figure 11 is provided in Figure 12 in connection with an exemplary data transfer. As noted with the other timing diagrams, there is no implied relationship between the time periods T1-Tn illustrated in Figure 12 and the same or similar time periods appearing in other timing diagrams of this  
30 disclosure. The 250MHz clock CLK250 116 and the 500 MHz clock CLK500 118 are



depicted at the top of Figure 12. Below these two waveforms are the two data core signals received by data transmit logic 112 from processing core 102, DATA0\_CORE 236 and DATA1\_CORE 232. Two bits of data are illustrated, bits D0 and D2 at time periods T1 and T2 on DATA0\_CORE 236 and bits D1 and D3 at time periods T1 and T2 on DATA1\_CORE 232.

D0 and D2 are latched on the next falling edge of CLK250, as shown by D0\_250\_LA 1122. Similarly, D1 and D3 are latched on the next falling edge of CLK250, as shown by D1\_250\_LA 1124. D1\_250\_LA 1124 is latched at the next rising edge of CLK500 118 to output D1\_5000\_LA 1126.

DATA\_MUX\_SELECT 1120 is a 250 MHz pulse synchronized with CLK500 116 and is generated by latching the 250 MHz clock using the falling edge of the 500 MHz clock. Thus, DATA\_MUX\_SELECT 1120 rises on the falling edge of CLK500 118. DATA\_SELECT 1128 illustrates the selection of either signal 1122 or 1126 as DATA\_MUX\_SELECT 1120 toggles. DATA\_SELECT 1128 is latched into a flip-flop 1110 on the falling edge of CLK500 118 due to the inverter 118 inverting CLK500 118. This results in the DATA\_OUT signal 234 illustrated in Figure 12, which is the same as that depicted in Figure 2B. Thus, data transmit logic 112 transmits the received data over a DATA\_OUT signal 234 at 500 MHz. By transmitting the data signal at twice the frequency as the differential data strobe signals, this aspect of the present invention cause the data and data strobe signals to experience a logic state transmission at the same time and at the same frequency, here, each rising edge of the higher frequency, or every 500 MHz.

#### **E. Source Synchronous Link Receiver 110**

Figure 10 is a schematic block diagram of one embodiment of source synchronous receiver 110. Source synchronous receiver 110 receives DATA\_OUT 234 and differential data strobe signals DS\_OUT 210 and DSN\_OUT 212. Differential data strobe DS\_OUT 210 and DSN\_OUT 212 are 250MHz clock signals while DATA\_OUT 234 transmits data at 500 MHz. That is, during each period of the differential data strobe 122, 2 bits of data are received by source synchronous receiver 110. This is referred to as

being “double pumped” in that two bits of data rather than one are transmitted during each clock cycle. As noted, this provides the advantage of providing a data signal that transitions with each transition of the differential data strobe 122.

DATA\_OUT 234 is received by a receiver 1012 and passed through a multiplexer 100. Multiplexer 1006 selects either DATA\_OUT 234 or an unrelated signal based on criteria not-relevant to the present invention. Similarly, DS\_OUT 210 and DSN\_OUT 212 are received by receivers 1014 and 1016 and passed through multiplexers 1008 and 1010. Multiplexers 1008 and 1010 are controlled similarly.

DS\_OUT 210 is used to latch data capture flip-flop 1002A while DSN\_OUT 212 is used to latch data capture flip-flop 212. Thus 2 bits of data are latched with each data strobe clock cycle. The rising edge of the differential data strobe DS\_OUT 210 clocks flip-flop 1002 while the rising edge of DSN\_OUT 212 clocks flip-flop 1002B. With this approach, the data capture flip-flops latch in 2 bits of data in a single data strobe cycle; that is 2 bits per 250 MHz, or 500 MHz.

The received data signal is passed through a delay and fan-out tree 1004 that induces delay in the data signal. As noted, in one embodiment, the differential data strobe is used to clock 18 pairs of data capture flip-flops 1002 since there are 18 data lines similar to that which carries DATA\_OUT 234. This distribution of the differential data strobe 122 imparts delay in DS\_OUT 210 and DSN\_OUT 212 that is not experienced by DATA\_OUT 234. Delay and fanout tree 1004 increases the delay experienced by the data signal 234 so that the buffering of the data signal and differential data 122 strobe are matched; that is, the differential data strobe is out of phase with the data strobe; that is, the edge of the differential data strobe occurs in the middle of the data eye. This insures the DATA\_OUT signal 234 is stable before latched into data capture flip-flops 1002.

In accordance with one aspect of the invention, DATA\_OUT 234 and differential data strobe signals DS\_OUT 210 and DSN\_OUT 212 are processed through the same logical and physical components in source synchronous receiver 110. Thus, driver 1012 is identical to driver 1014 and 1016. Similarly, multiplexer 1006 is identical to multiplexer 1008 and 110, and the select line is driven by the same local clock. For the reason set forth above, in certain implementations of source synchronous receiver 110, a

delay and fanout tree 1004 is implemented to compensate for delays across such receivers. As noted, this insures injected link noise is experienced by both, DATA\_OUT signal 234 and the differential data strobe signals 122.

Figure 13 is a flow chart of the processes performed in accordance with one embodiment of the present invention to halt a differential data strobe transmitted on a source synchronous link 100.

At block 1302 the transmitter is transmitting a differential data strobe signal in normal operating mode. That is, the differential data strobe is two opposing phase clock signals transmitted at a first clock frequency over two clock clines of a communication link 106. The data strobe signals alternate between a high logical state and a low logical state during each cycle of the data strobe signal.

At block 1304 the source synchronous transmitter receives a command from a host processing core to halt the differential data strobe signal 122. Preferably, the logical state in which the data strobe will be halted can be specified, in which case the transmitter determine what that logical state is at block 1306.

In response to the halt request and, perhaps, the logic level specification, at block 1306 the source synchronous transmitter maintains the differential data strobe signals transmitted by the transmitter at one of either the high logical state or the low logical state.

This continues indefinitely until the transmitter receives a request to resume normal data strobe transmissions, in which case processing continues at block 1302.

Further features of the present invention are described in commonly-owned U.S. Utility Patent Application entitled "A SOURCE SYNCHRONOUS LINK WITH DATA AND CLOCK SIGNALS HAVING THE SAME ELECTRICAL CHARACTERISTICS" naming as inventors Karen Lo, Jeffery A. Benis and Allan R. Desroches, filed concurrently herewith under Attorney Docket No. 10002534-1, the specification of which is herein incorporated by reference.

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not

limitation. Thus, the breadth and scope of the present invention are not limited by any of the above-described exemplary embodiments, but are defined only in accordance with the following claims and their equivalents.

What is claimed is:

Variable	Mean	Standard deviation	Minimum	Maximum
Age	34.2	10.5	22	55
Gender	0.5	0.5	0	1
Marital status	0.6	0.5	0	1
Education	12.5	1.5	10	15
Income	15.2	5.8	10	25
Health status	0.8	0.4	0	1
Employment status	0.7	0.5	0	1
Living arrangement	0.9	0.3	0	1
Religious affiliation	0.6	0.5	0	1
Political affiliation	0.5	0.5	0	1
Volunteer status	0.4	0.5	0	1
Charitable giving	0.3	0.4	0	1
Community involvement	0.5	0.5	0	1
Life satisfaction	0.7	0.4	0	1
Overall well-being	0.6	0.5	0	1

**CLAIMS**

- 1 1. A source synchronous link comprising:  
2 a communication link;  
3 a source synchronous receiver coupled to said communication link; and  
4 a source synchronous transmitter coupled to said communication link, including,  
5 data transmit logic configured to manage the transmission of data signals  
6 over a data line of said communication link; and  
7 data strobe transmit logic configured to generate a one or more data strobe  
8 signals over a clock line of said communication link, wherein said data strobe  
9 transmit logic halts each said one or more data strobe signals in a logical state in  
10 response to an external condition.
- 1 2. The source synchronous link of claim 1, wherein said one or more data strobe  
2 signals comprise a first data strobe signal and a second data strobe signal transmitted  
3 with a phase opposite a phase of said first frequency.
- 1 3. The source synchronous link of claim 1, wherein said first data strobe signal and said  
2 second data strobe signal may be transmitted at either one of two logical states and  
3 wherein said data strobe transmit logic maintains said first data strobe signal at a first of  
4 said two logical states and maintains said second data strobe signal at a second of said  
5 two logical states when said data strobe transmit logic halts said one or more data strobe  
6 signals.
- 1 4. A source synchronous transmitter constructed and arranged to transmit a differential  
2 data strobe over a source synchronous link at a first frequency, with the differential data  
3 strobe signals toggling between one of two logical states at said first frequency when  
4 operating in a normal mode of operation and with the differential data strobe signals held  
5 at one of the logical states when operating in a data capture debug mode of operation.

1 5. A debug system to determine whether source synchronous receiver has properly  
2 captured data transmitted from a transmitter, comprising:  
3 a source synchronous transmitter;  
4 a source synchronous receiver;  
5 a debug system configured to control said transmitter to transmit data and a data strobe at  
6 a first frequency and to transmit a debug bit pattern while holding said differential data  
7 strobe at a predetermined logic level;  
8 a data capture storage and analysis device configured to scan said receiver to retrieve and  
9 store captured data for comparison with said debug bit pattern.

1 6. The source synchronous link of claim 4, wherein said transmitter comprises:  
2 a differential data strobe transmit logic configured to generate said differential data  
3 strobe comprising a data strobe signal and an inverse data strobe signal;  
4 a differential data strobe signal generator configured to determine a said logical states of  
5 said data strobe and said inverse data strobe signals;  
6 a strobe stopping logic that controls said logic level signals utilized by said signal  
7 generator to cause said data strobe and said inverse data strobe signals to remain halted in  
8 a desired logical state.

1 7. In a source synchronous communication system, a method for determining whether a  
2 source synchronous link receiver properly captured data transmitted by a source  
3 synchronous transmitter, the method comprising the steps of:  
4 a) transmitting by the transmitter a data signal at a first clock frequency;  
5 b) transmitting by the transmitter concurrently with said step a), at least one data strobe  
6 signal at a second clock frequency, wherein said data strobe signal alternates between a  
7 high logical state and a low logical state during each data strobe cycle;  
8 c) receiving, by the transmitter, a command to halt the data strobe signal; and  
9 d) maintaining, by the transmitter in response to said command, said one or more data  
10 strobe signals transmitted by said transmitter at one logical state.

1 8. The method of claim 7, further comprising the step of:  
2 e) prior to said step d), receiving an indication of the logical state in which to maintain  
3 said data strobe signal, and  
4 wherein said one logical state at which said one or more data strobe signals are held, is  
5 said logical state indicated in said step e).

1 9. In a source synchronous system, a method for determining whether a source  
2 synchronous receiver has properly captured data transmitted from a source synchronous  
3 transmitter, the method comprising the steps of:  
4 selecting a bit pattern to transmit over communication link coupling said transmitter  
5 and said receiver;  
6 causing the transmitter to halt differential data strobe and to transmit concurrently  
7 said predetermined bit pattern to the receiver;  
8 scanning data capture flip-flops in the source synchronous receiver to retrieve  
9 captured bit pattern;  
10 storing said captured data; and  
11 comparing said captured data with said transmitted bit pattern.

1 10. The method of claim 9, wherein said step of selecting comprises the steps of:  
2 writing said predetermined bit patterns to a memory; and  
3 retrieving a selected predetermined bit pattern from the memory.

1 11. A differential data strobe transmitter for generating a differential data strobe  
2 comprising a data strobe signal and an inverse data strobe signal over a communication  
3 link with a data signal, comprising:  
4 a differential data strobe signal generator that determines a shape of said data  
5 strobe signal and said inverse data strobe signal waveforms; and  
6 strobe stopping logic configured to control signal level states used by said signal  
7 generator logic to cause said data strobe signal and said inverse data strobe signal to  
8 remain halted in a desired logical state.

1 12. The differential data strobe transmitter of claim 11, wherein said differential data  
2 strobe signal generator logic selects alternately between two applied signal levels to  
3 generate each said data strobe signal and said inverse data strobe signal.

1 13. The differential data strobe transmitter of claim 12, wherein said differential data  
2 strobe signal generator receives as inputs a first and a second logic level signal for  
3 selection to generate said data strobe signal and a third and fourth logic level signals for  
4 selection to generate said inverse data strobe signal.

1 14. The differential data strobe transmitter of claim 12,  
2 wherein during normal operations, said differential data strobe is not halted, said  
3 first and third input signals are held consistently in an asserted state while said second of  
4 fourth input signals are held consistently in a de-asserted state,  
5 wherein said signal generator selects alternately said first and said second input  
6 signals to generate said data strobe signal at a first clock frequency, and between said  
7 third and said fourth input signals to generate said inverse data strobe signal at said first  
8 clock frequency.

1 15. The differential data strobe transmitter of claim 12, wherein said data strobe signal  
2 and said inverse data strobe signal are each generated as single ended bits that are  
3 opposite in phase with each other.



**ABSTRACT**

Methods and apparatus for halting the data strobes transmitted over a source synchronous link to enable the data stored in the data capture flip-flops in a source synchronous receiver to be scanned out for subsequent analysis. This allows for the  
5 evaluation of the captured data without placing additional components in the functional data path and, therefore, without increasing the latency of the transmission. To provide optimal timing margins the data and data strobe paths are logically and electrically matched. This includes routing the data and data strobe signals in close proximity from the transmitter to the receiver, and through the same logical and physical elements in the  
10 transmitter and receiver. This insures that any injected link noise is experienced common-mode. In addition, the data strobe signal is preferably driven at one-half of the period of the data signal so that the data strobe and data signals experience logical state transitions at the same time and at the same frequency. This insures maximally similar electrical modes on the communication link, further maximizing link margin.

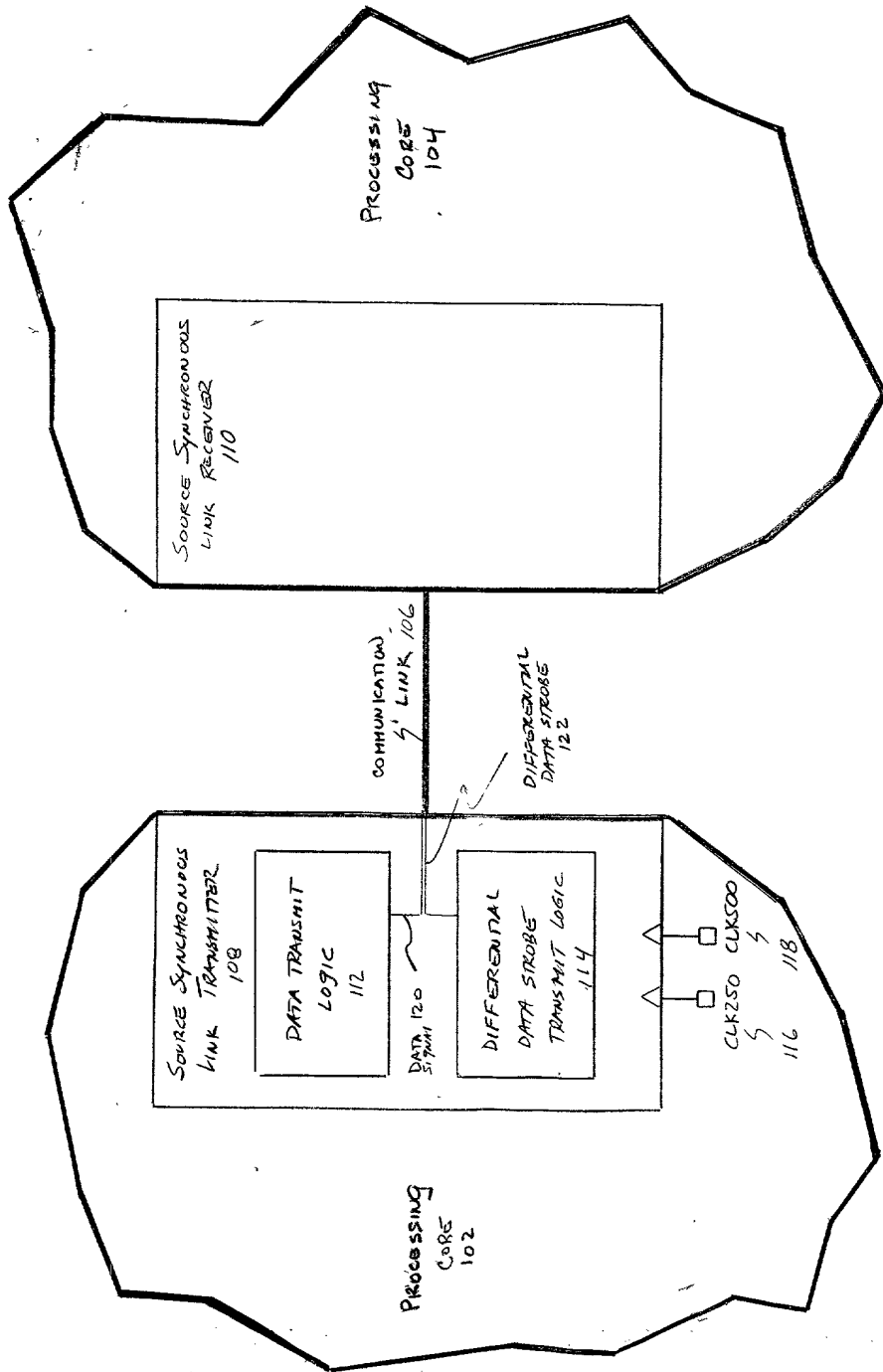


FIGURE 1A SOURCE SYNCHRONOUS LINK 100



00000000

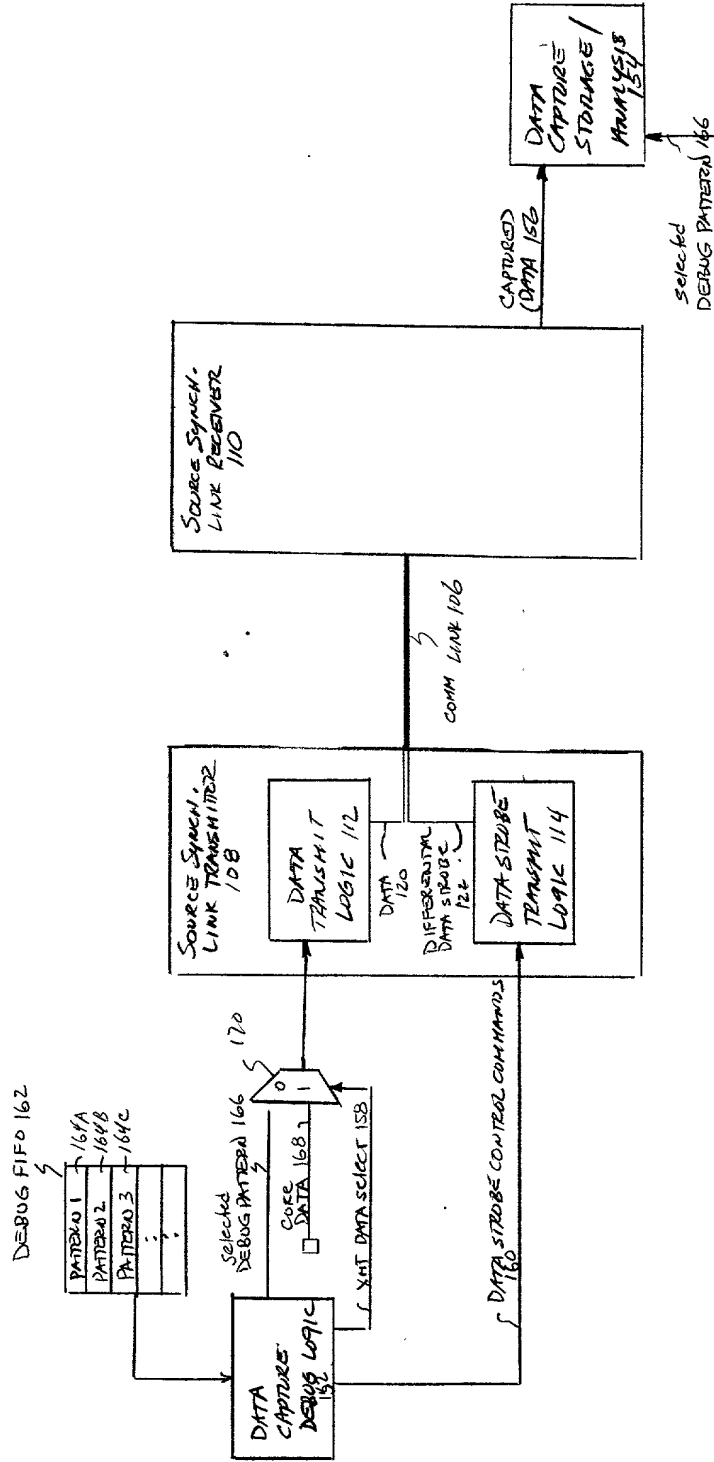


FIGURE 1B

DATA CAPTURE DEBUG  
SYSTEM 150

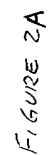


FIGURE 2A

22-144 100 SHEETS  
 22-144 100 SHEETS  
 22-144 200 SHEETS  
 22-144 200 SHEETS  
 22-144 200 SHEETS  
 22-144 200 SHEETS

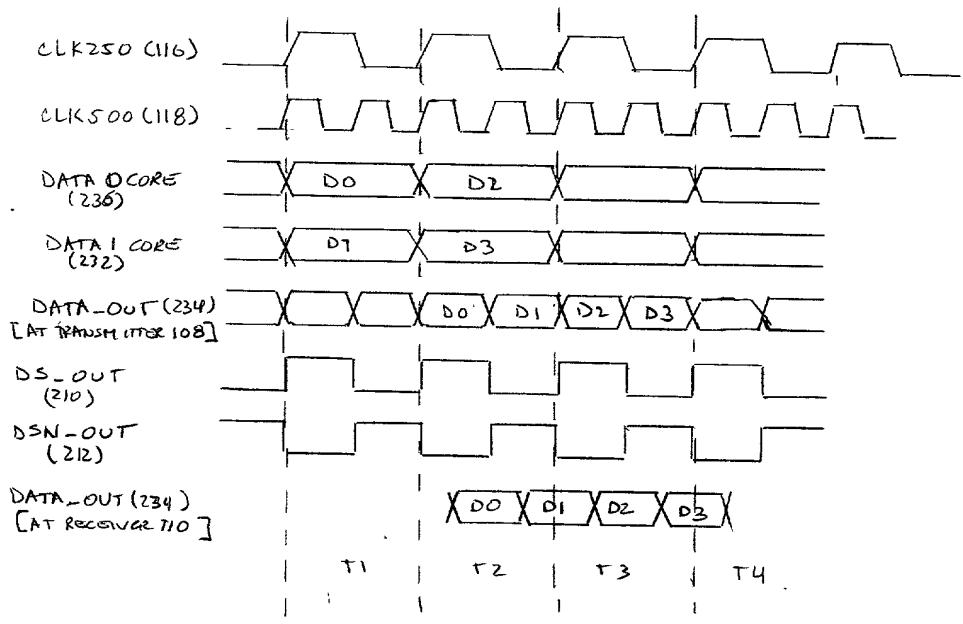


FIGURE 2B

DATA AND DATA STROBE  
 SIGNAL RELATIONSHIPS  
 200

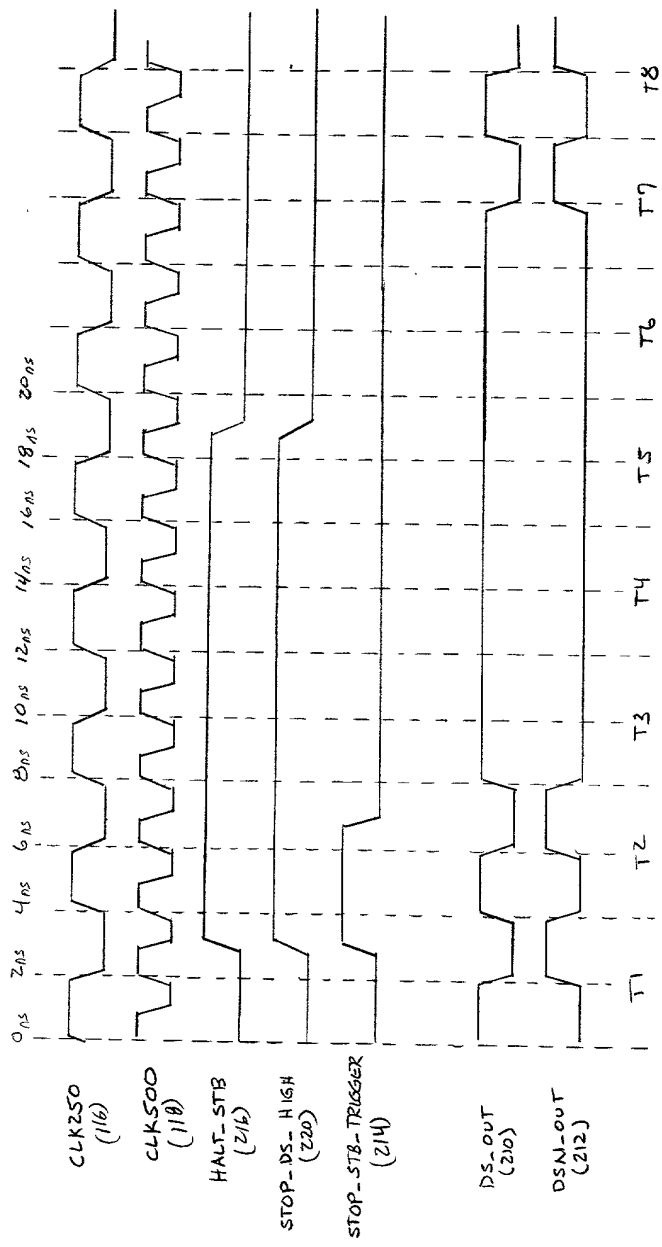
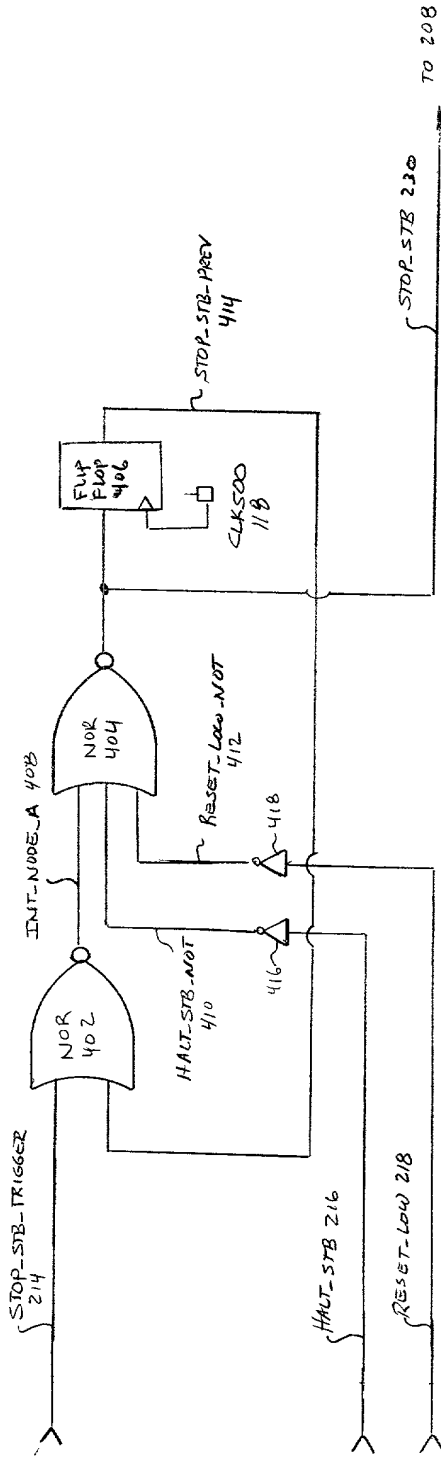


FIGURE 3

Transmit Logic  
Input/output signal  
Relationships 300



PULSE STRETCH LOGIC 206

FIGURE 4

22-142 100 SHEETS  
 22-142 100 SHEETS  
 22-144 200 SHEETS  
 22-144 200 SHEETS

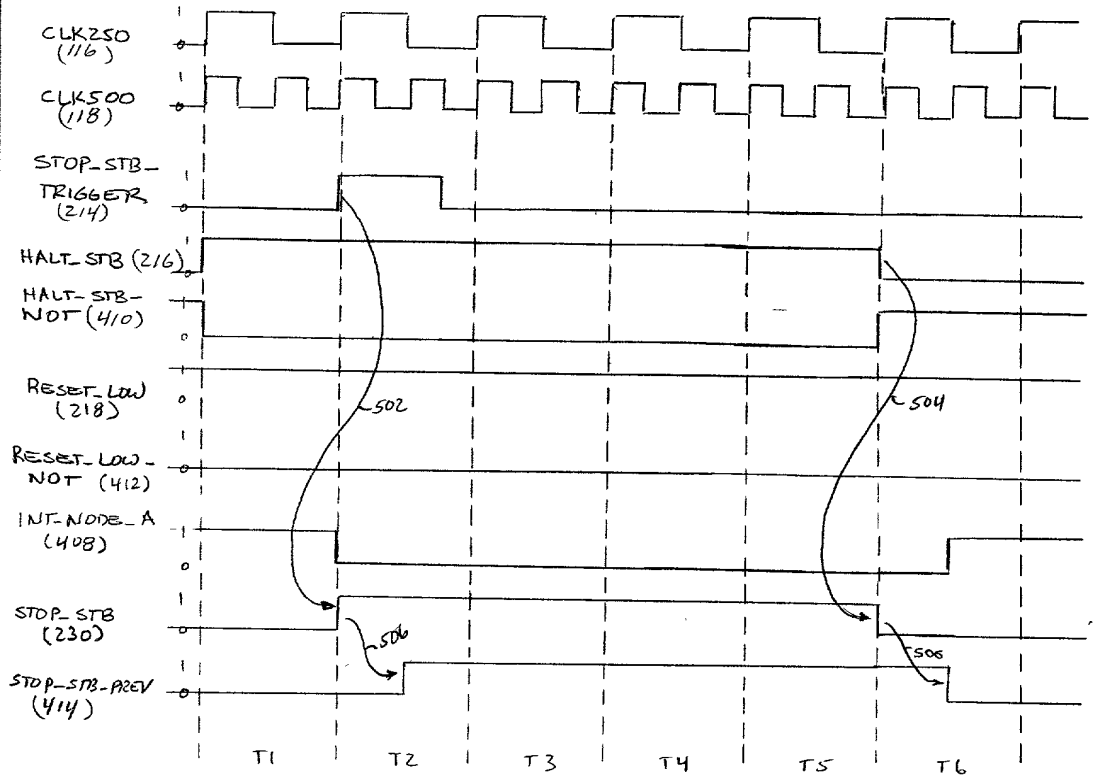


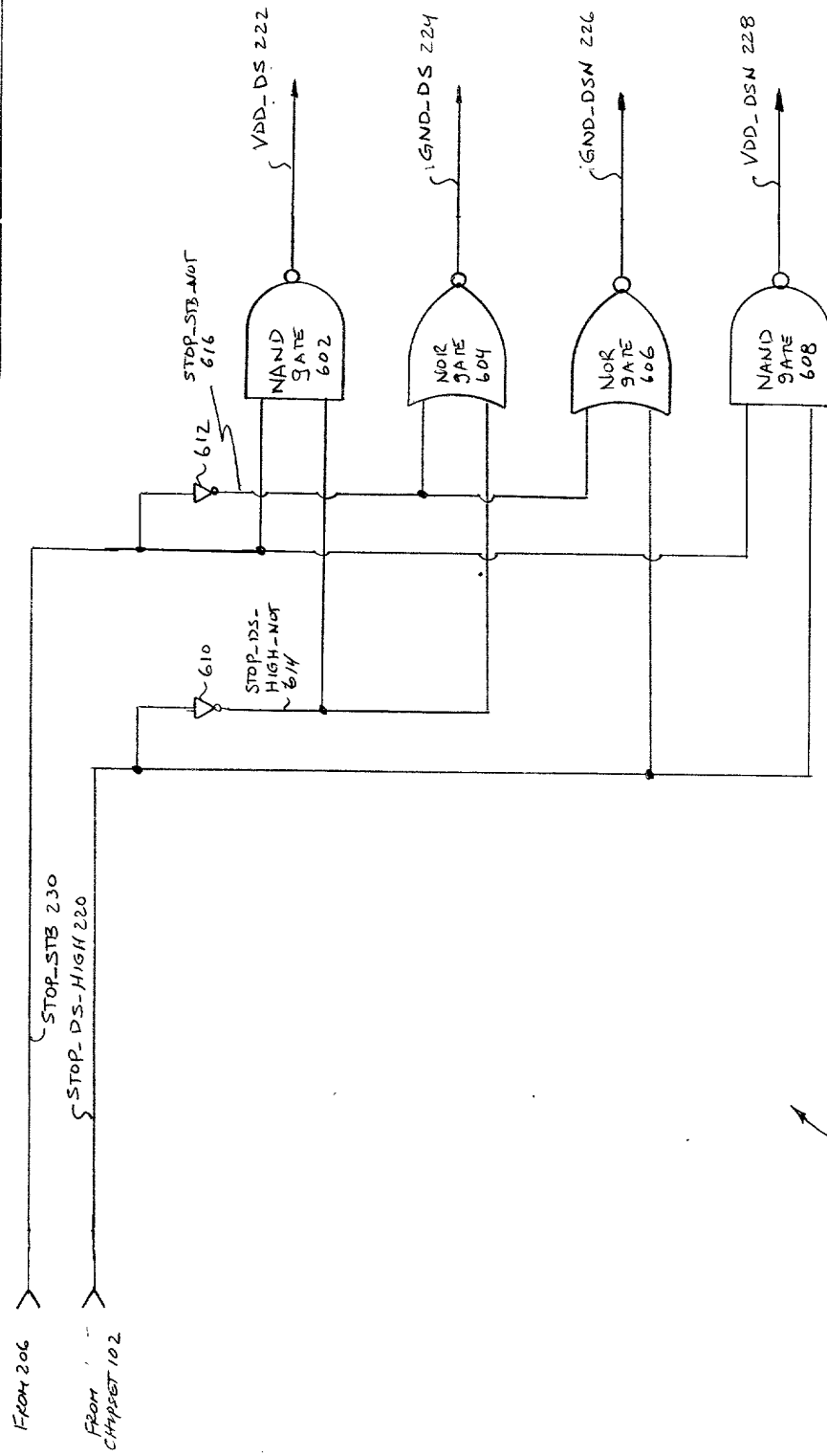
FIGURE 5

↑  
 PULSE STRETCH LOGIC  
 TIMING RELATIONSHIPS  
 500



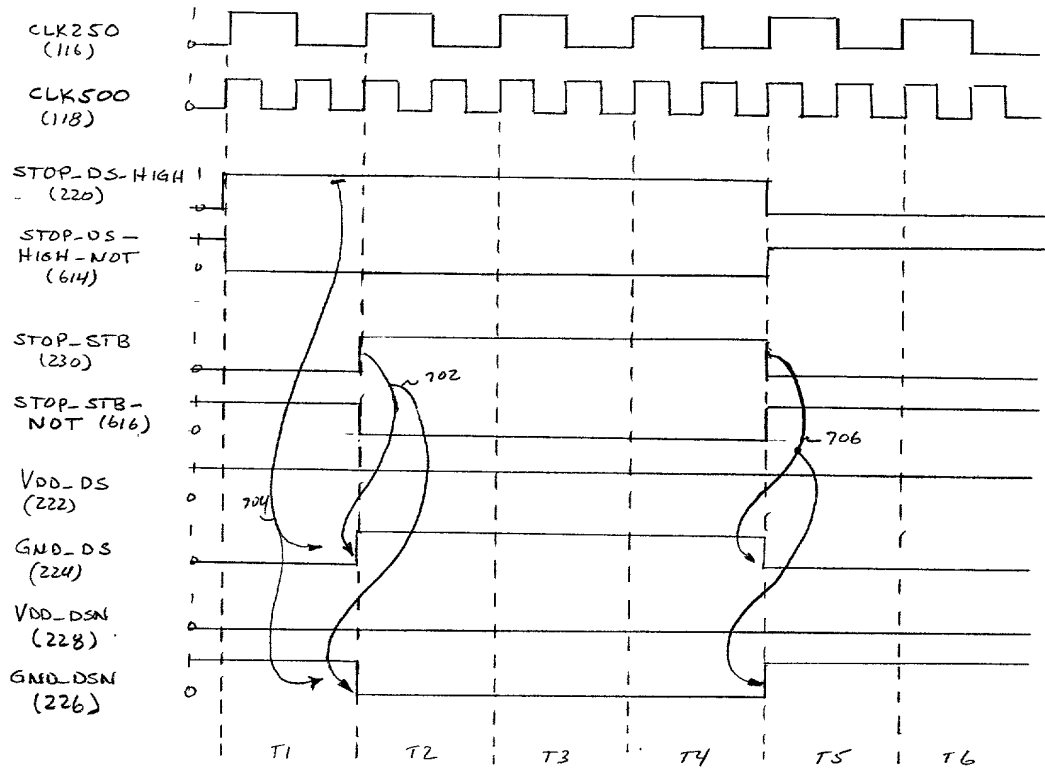


008-40



DIFFERENTIAL DATA STROBE  
CONTROL LOGIC 208

FIGURE 6



DIFFERENTIAL DATA STROBE  
 CONTROL TIMING  
 RELATIONSHIPS 700

FIGURE 7

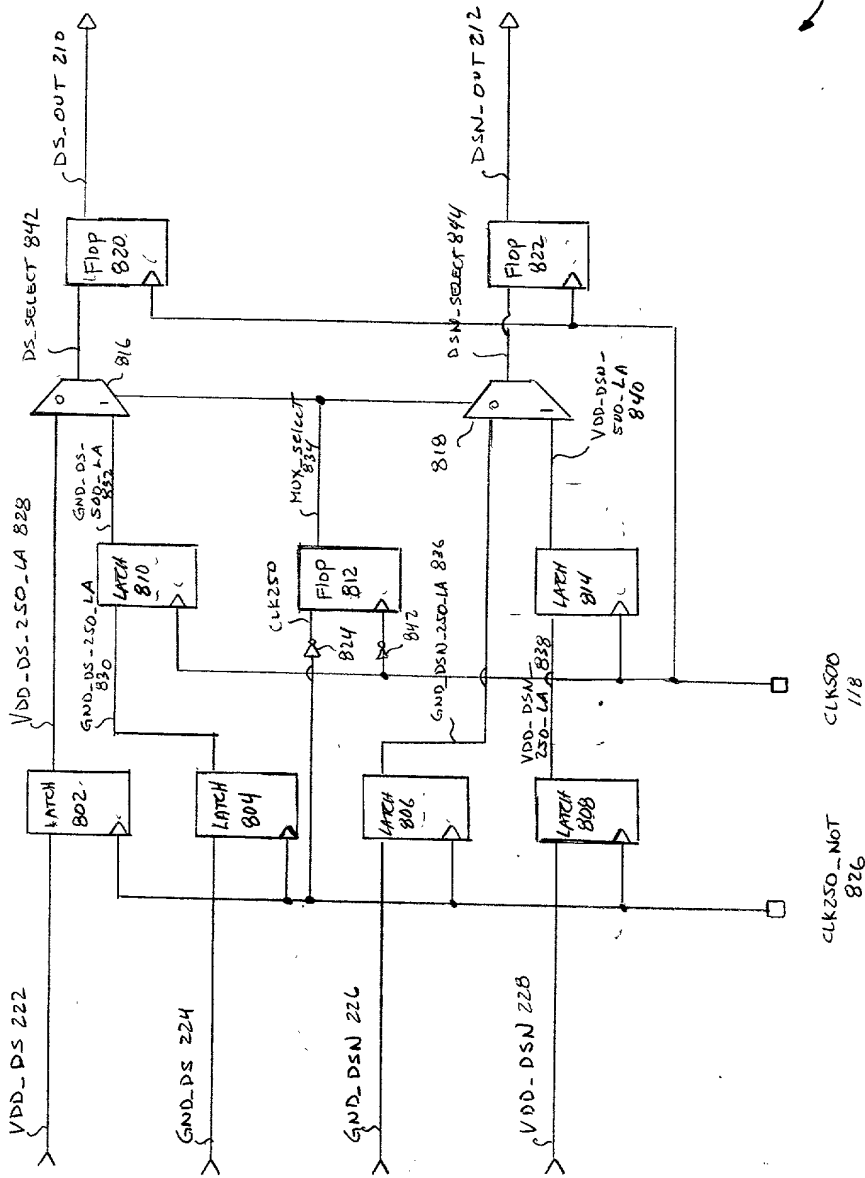


FIGURE 8

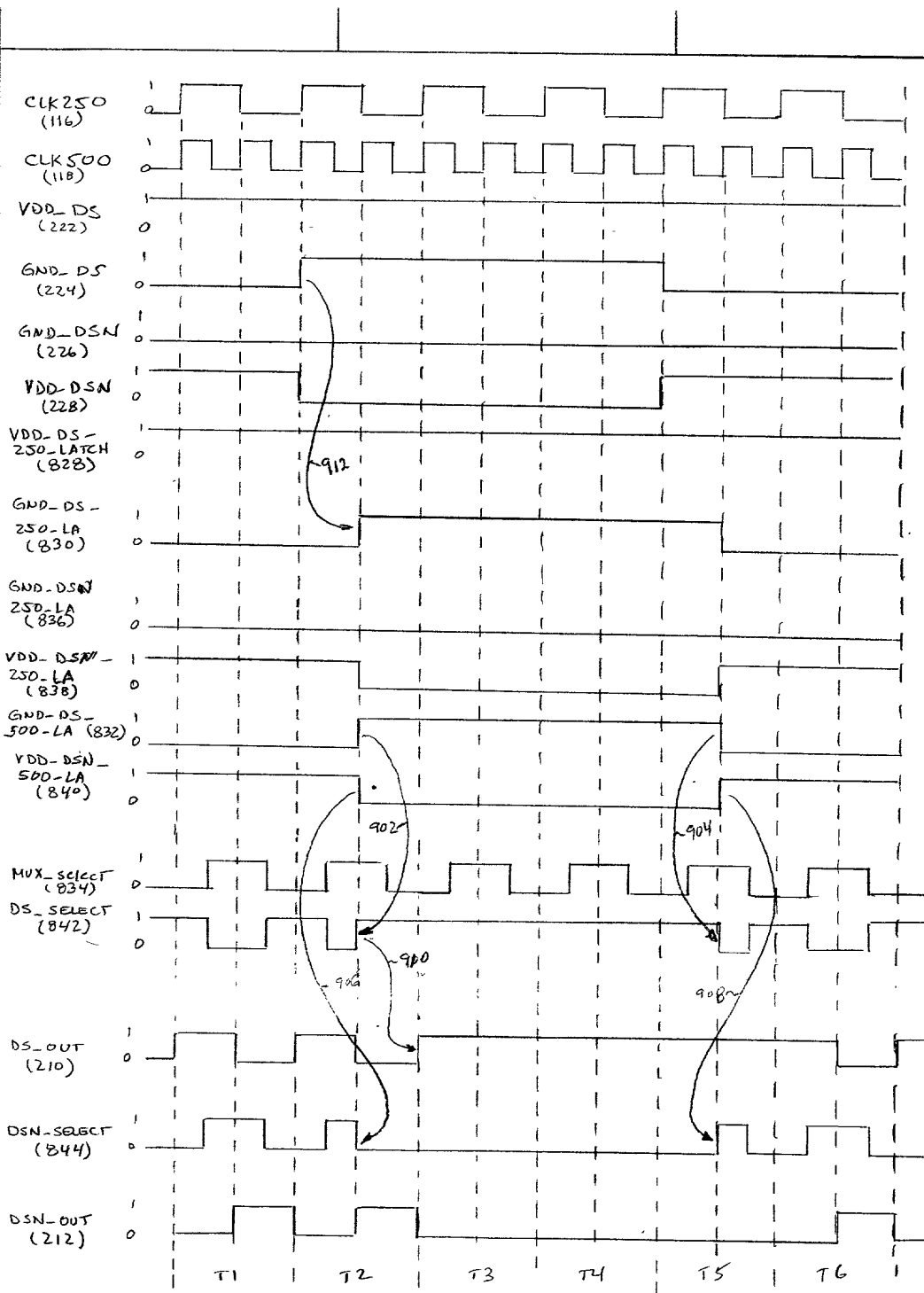
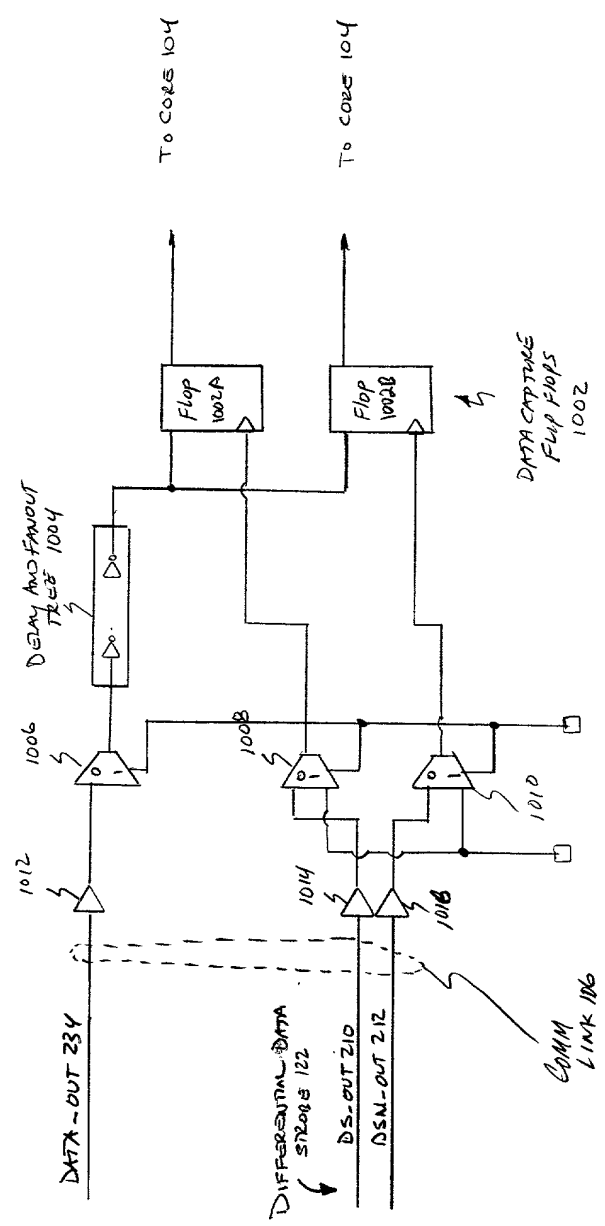


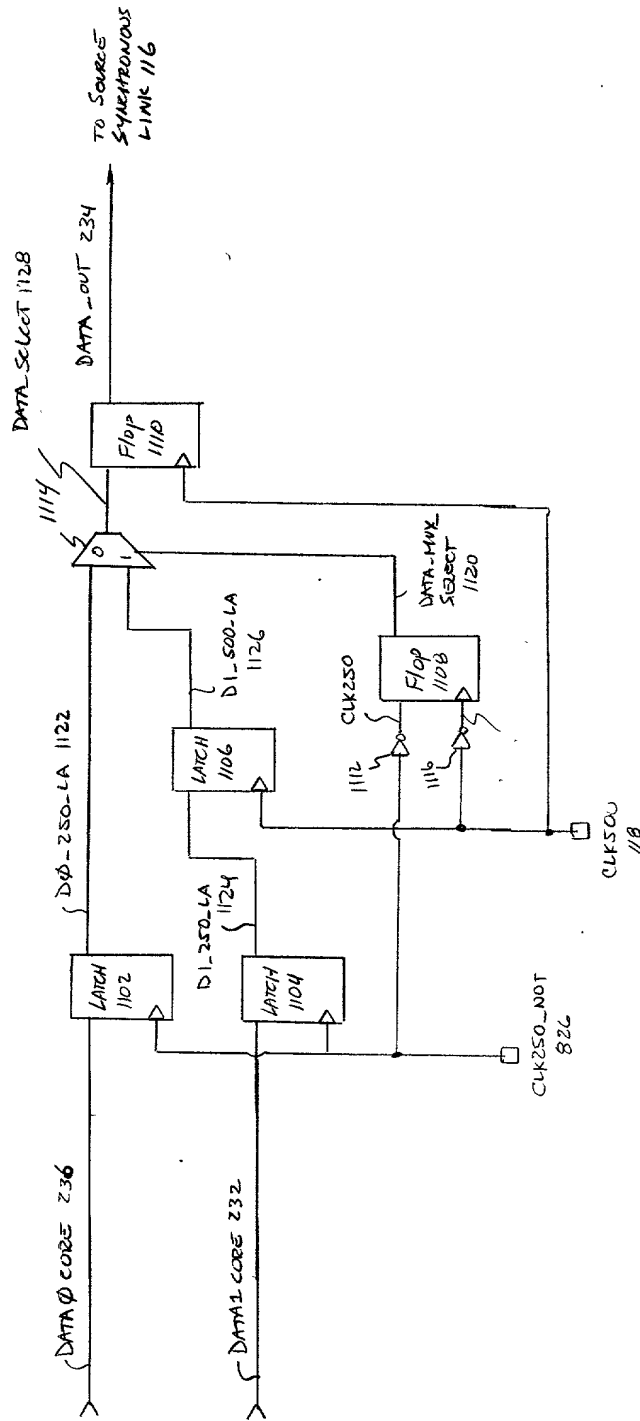
FIGURE 9

DIFFERENTIAL DATA  
STROBE SIGNAL GEN.  
TIMING RELATIONS P.5  
900



SOURCE SYNCHRONOUS  
 RECEIVER 110

FIGURE 10



DATA TRANSMIT  
Logic 112

FIGURE 11

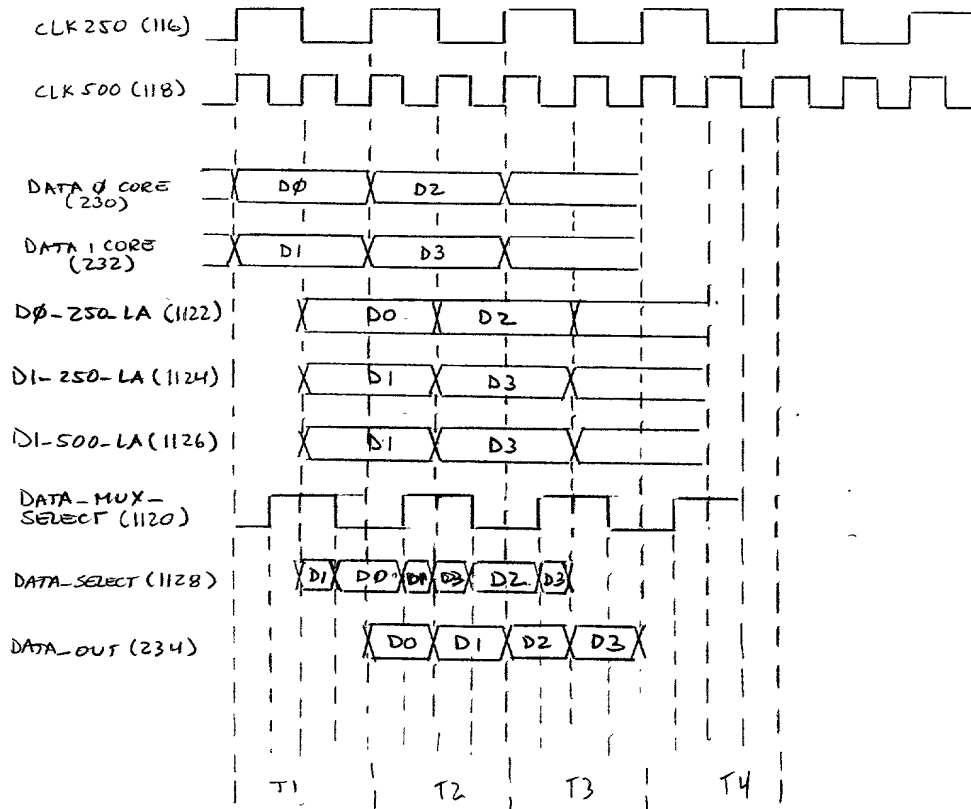


FIGURE 12

DATA TRANSMIT  
SIGNAL RELATIONSHIPS  
1200

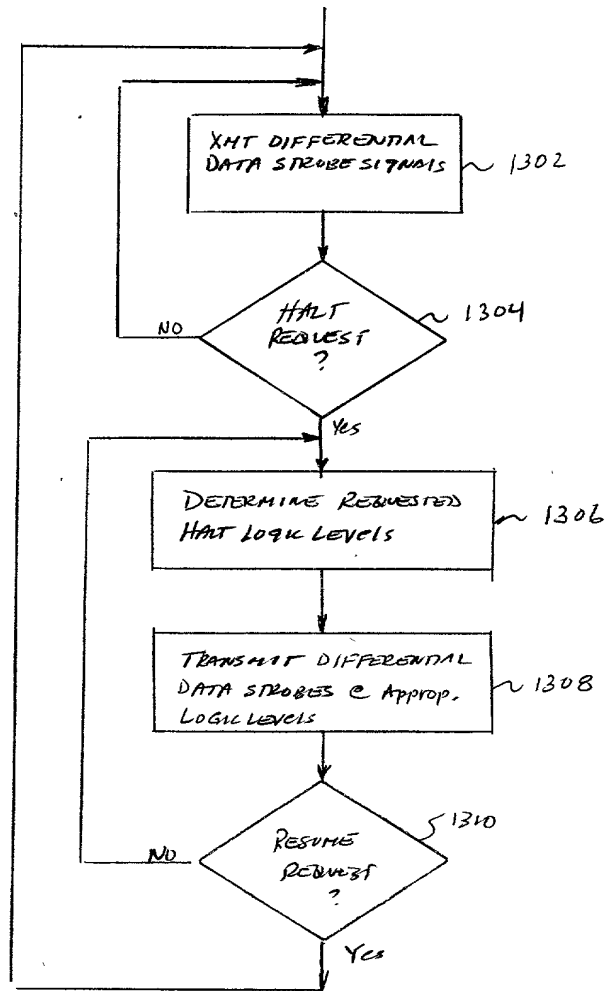


FIGURE 13



**DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION**ATTORNEY DOCKET NO. 10002496-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**HALTING DATA STROBES ON A SOURCE SYNCHRONOUS LINK AND UTILIZATION OF SAME TO  
DEBUG DATA CAPTURE PROBLEMS**

the specification of which is attached hereto unless the following box is checked:

( ) was filed on \_\_\_\_\_ as US Application Serial No. or PCT International Application  
Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

**Foreign Application(s) and/or Claim of Foreign Priority**

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: _____ NO: _____
			YES: _____ NO: _____

**Provisional Application**

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

**U. S. Priority Claim**

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

**POWER OF ATTORNEY:**

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Customer Number **022879**Place Customer  
Number Bar Code  
Label hereSend Correspondence to:  
**HEWLETT-PACKARD COMPANY**  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, Colorado 80528-9599**Direct Telephone Calls To:****Michael G. Verga**  
**(617) 244-0490**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature \_\_\_\_\_

Date \_\_\_\_\_

**DECLARATION AND POWER OF ATTORNEY  
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Inventor's Signature \_\_\_\_\_

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Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature \_\_\_\_\_

Date \_\_\_\_\_

Full Name of # 8 joint inventor: \_\_\_\_\_

Citizenship: \_\_\_\_\_

Residence: \_\_\_\_\_

Post Office Address: \_\_\_\_\_

Inventor's Signature \_\_\_\_\_

Date \_\_\_\_\_